fail - safe function (Fail - Safe) slew rate limited

RS-485 transceiver

Chip overview

The BL3085A is a low-power transceiver for RS-485 communication, with one driver and one receiver in each device . The chip contains a fail-safe circuit to ensure that the output of the receiver is in a logic high state when the input of the receiver is open or short-circuited . The BL3085A features a slew-rate-limited driver that reduces EMI and reduces reflections caused by improperly terminated cables, enabling error-free data transmission up to 250kbps . The BL3085A has a high receive input impedance, making it possible to support up to 256 transceivers on the bus. The transceiver end of BL3085A has +/-10kV anti-static capability.

Chip pin logic diagram and description

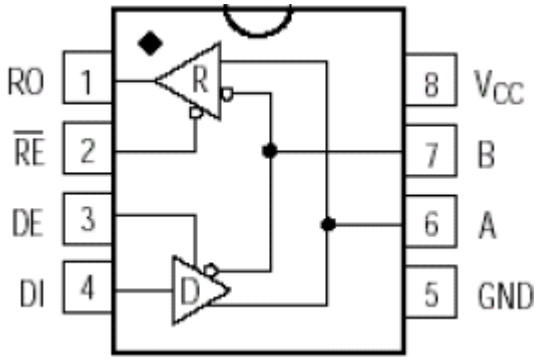


Figure 1: BL3085A pin logic diagram

Application field

- industrial control
- Electricity meter, water meter, gas meter

- security system
- Lighting system

Chip pin description

pin	name	function
1	RO	receiver output.
2	/RE	Receiver output enable. RO output is valid when /RE is low; when /RE is high, RO to a high-impedance state.
3	DE	Driver output enable. The driver output is valid when DE is high, and the output is high-impedance when DE is low.
4	DI	drive input.
5	GND	grounded.
6	A	receiver input and driver output.
7	B	receiver input and driver output.
8	V_{CC}	power input.

Send and Receive Truth Tables

发送				
输入			输出	
/RE	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

接收			
输入		输出	
/RE	DE	A-B	RO
0	X	≥-0.04V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Typical application circuit diagram

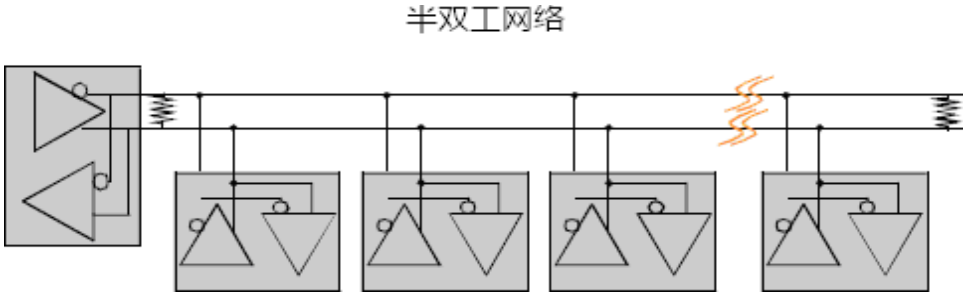


Figure 2. Typical application circuit diagram of BL3085A

absolute maximum

parameters	the symbol	size	unit
supply voltage	V_{CC}	+7	V
Control input voltage	/RE, DE	-0.3 to V_{CC} +0.3	V
Driver input voltage	DI	-0.3 to V_{CC} +0.3	V
Driver output voltage	A, B	-8~+13	V
Receiver input voltage	A, B	-8~+13	V
Receiver output voltage	RO	-0.3 to V_{CC} +0.3	V
range of working temperature		-40 ～ +85	℃

DC Electrical Characteristics

（V_{CC}=+5V±5%, TA= - 40℃ ~ + 85℃, typical value at V_{CC}=+5V, TA = 25°C）(Note 1)

parameter	symbol	Test Conditions		the smallest	typical	maximum	unit
Working voltage range	Vcc			4.5		5.5	V
driver							
Differential Driver Output (no load)	V_{OD1}	Figure 3				5	V
Differential Driver Output	V_{OD2}	Figure 3, R=27Ω		1.5			V
The magnitude of the differential output voltage variezation (Note 2)	ΔV_{OD}	Figure 3, R=27Ω				0.2	V
Driver Common Mode Output Voltage	VOC	Figure 3, R=27Ω				3	V
Amplitude variation of common mode voltage (Note 2)	ΔV_{OC}	Figure 3, R=27Ω				0.2	V
input high voltage	V_{IH1}	DE,DI,/RE		2.0			V
input low voltage	V_{IL1}	DE,DI,/RE				0.8	V
DI input hysteresis	V_{HYS}				100		mV
Input Current Half Duplex	I_{IN4}	DE=GND VCC = GND or 5.25V	V_{IN}=12V			125	μA
			V_{IN}=-7V			-75	
Driver short circuit output current (Note 3)	I_{OSD}	-7V ≦ V_{OUT} ≦ V_{CC}		-250			mA
		0V ≦ VOUT ≦ 12V				250	
		0V ≦ V_{OUT} ≦ V_{CC}		±25			
receiver							
Receiver Differential Threshold Voltage	VTH	-7V ≦ VCM ≦ 12V		-200	-125	-40	mV
Receiver Input Skew	ΔV_{TH}				40		mV
Receiver output high voltage	V_{OH}	I_O=-4mA, V_{ID}=-50mV		V_{CC}-1.5			V
Receiver output low voltage	V_{OL}	I_O=4mA, V_{ID}=-200mV				0.4	V
Receiver Tri-State Output Current	QUR	0.4V ≦ VO ≦ 2.4V				±1	μA

Receiver input impedance	R_{IN}	-7V ≦ VCM ≦ 12V		96			KΩ
Receiver output short circuit current	OSR	0V ≦ V_{RO} ≦ V_{CC}		±7		±95	mA
supply current							
supply current	I_{CC}	No load , /RE=DI= GND or VCC	DE=V_{CC}		475	900	μA
			DE=GND		420	800	μA
Supply current in standby mode	I_{SHDN}	DE=GND, /RE=VCC , DI=V_{CC} or GND			0.1	10	μA

Note 1: All currents into the device are positive and all currents out of the device are negative; all voltages are to ground unless otherwise specified. Note 2: When DI input changes state, △ V_{OD} and △ V_{OC} V_{OD} and V_{OC} amount of change.

Note 3: Maximum current is used for peak current just before regenerative current limiting, minimum current is used during current limiting.

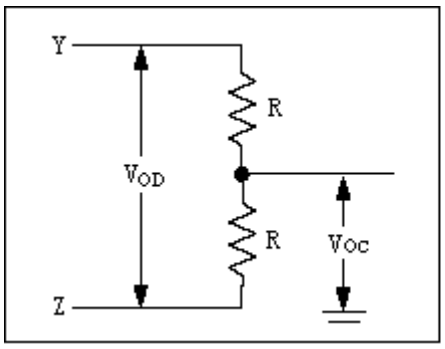
transmission characteristics

(V_{CC}=+5V±5%, TA= -40 ℃ ~ +85 ℃, the typical value is at V_{CC}=+5V , TA = 25 ℃)

parameter	symbol	condition	the smallest	typical	maximum	unit
Driver input to output	T_{DPLH}	Figures 5 and 7 , R_{DIFF} =54Ω C_{L1}=C_{L2} =100pF	250	720	2000	ns
	T_{DPHL}		250	720	1000	
Driver output $\|T_{DPLH} - T_{DPHL}\|$	T_{DHKEW}	Figures 5 and 7 , R_{DIFF} =54Ω C_{L1}=C_{L2} =100pF		-3	±100	ns
Driver Rise or Fall Time	T_{DR} , T_{DF}	Figures 5 and 7 , R_{DIFF} =54Ω C_{L1}=C_{L2} =100pF	200	530	750	ns
Maximum data rate	F_{MAX}		250			kbps
Driver Enable to Output High	TZH_	Figures 6 and 8 , C_L=100pF S2 off			2500	ns
Driver Enable to Output Low	QZL_	Figures 6 and 8 , C_L=100pF S1 off			2500	ns
Low to drive inactive time	DLZ_	Figures 6 and 8 , C_L=15pF S1 off			100	ns
High to drive invalid time	T_{DHZ}	Figures 6 and 8 , C_L=15pF S2 off			100	ns
receiver input to output	T_{RPLH} RPHL_	Figures 9 and 11 , $\|V_{ID}\| \geq 2.0V$ VID ≦ 15ns The rise and fall times of		127	200	ns
Differential Receiver $\|T_{DPLH} - T_{DPHL}\|$	T_{RSKD}	Figures 9 and 11 , $\|V_{ID}\| \geq 2.0V$ VID ≦ 15ns The rise and fall times of		3	±30	ns
Receiver Enable to Output Low	QUR_	picture 4 and 10 C_L=100pF S1 closure		20	50	ns
Receiver Enable to Output High	QUR_	picture 4 and 10 C_L=100pF S2 closure		20	50	ns
Receiver Low to Inactive Time	RLZ_	picture 4 and 10 C_L=100pF S1 closure		20	50	ns
Receiver High to Inactive Time	T_R	picture 4 and 10 C_L=100pF S2 closure		20	50	ns
Standby time	T_{SHDN}		50	200	600	ns

Driver Enable from Standby to Output High	$T_{DZH(SHDN)}$	Figures 6 and 8, C_L=15pF S2 off			4500	ns
Driven from standby to output low device enable	$T_{DZL(SHDN)}$	Figures 6 and 8, C_L=15pF S1 off			4500	ns
Receiver Enable from Standby to Output High	$T_{RZH(SHDN)}$	picture 4 and 10, C_L=100pF S2 closure			3500	ns
Receiver Enable from Standby to Output Low	$T_{RZL(SHDN)}$	picture 4 and 10, C_L=100pF S1 closure			3500	ns

Test circuit and switch characteristics



picture 3： Driver DC Test Load

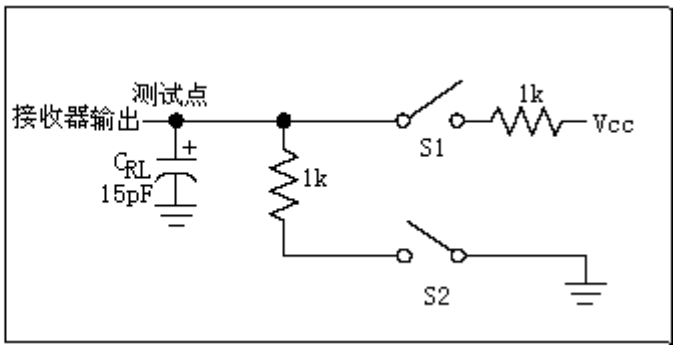


diagram 4： Receiver Enable/Disable Timing Test Load

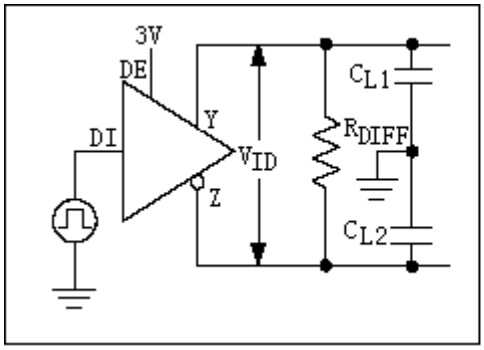


图 5：Driver Timing Test Circuit

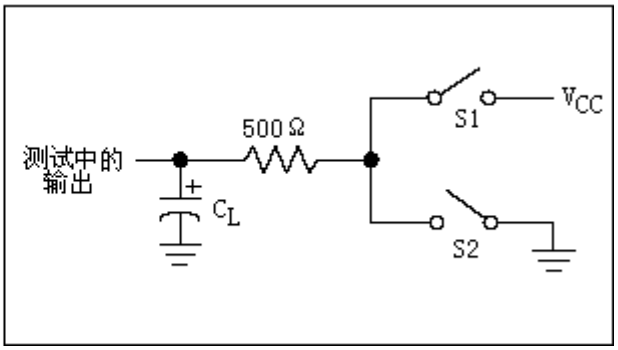


图 6：Driver Enable/Disable Timing test Load

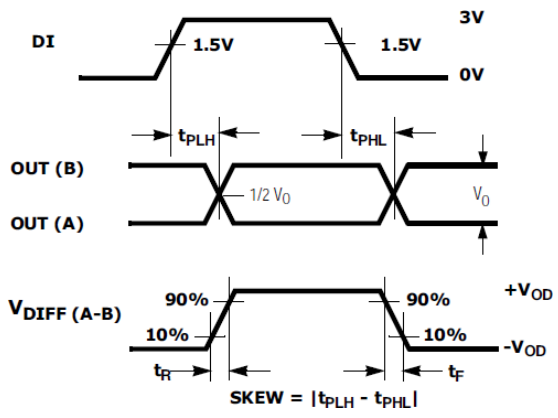


图 7：Driver Propagation Delays

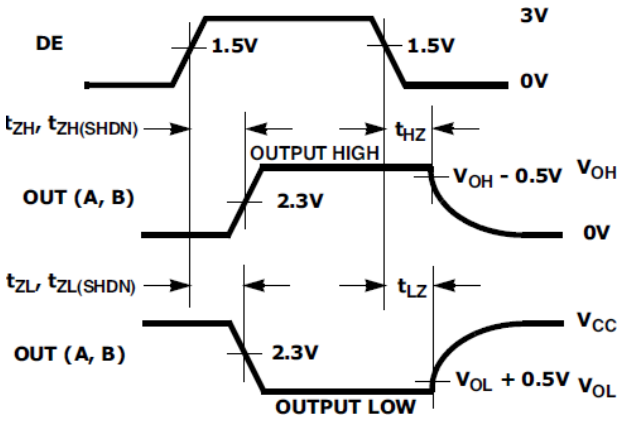
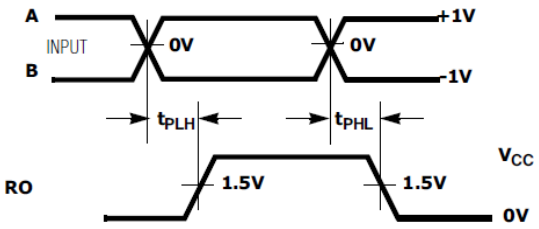


图 8：Driver Enable and Disable Times



picture 9： Receiver Propagation Delays

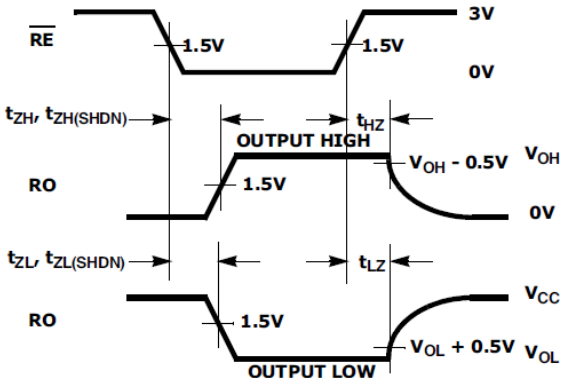


diagram 10： Receiver Enable and Disable Times

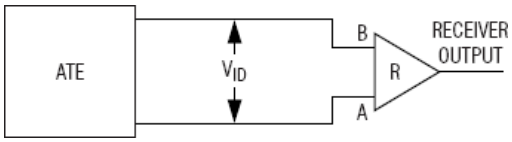
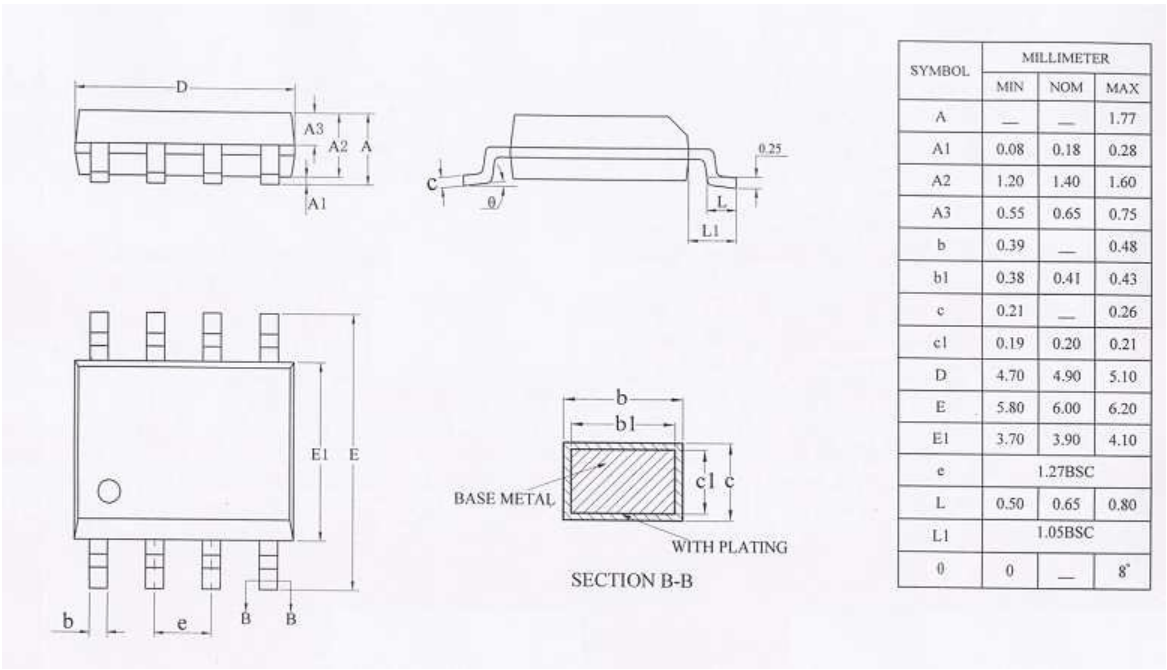


Figure 11： Receiver Propagation Delay Test Circuit

Package Information SOP8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	—	8°