EC200U Series

QuecOpen Hardware Design

LTE Standard Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

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1 Introduction

This document defines the EC200U series QuecOpen module and describes their air interfaces and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC200U series QuecOpen module. To facilitate its application in different fields, relevant reference design is also provided for customers' reference. Associated with application note and user guide, customers can use EC200U series QuecOpen module to design and set up mobile applications easily.

This document is applicable to following modules:

- EC200U-CN QuecOpen
- EC200U-EU QuecOpen

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, ANTCTL[0:3] refers to all four ANTCTL pins, ANTCTL0, ANTCTL1, ANTCTL2, and ANTCTL3.

2 Product Concept

2.1. General Description

EC200U series QuecOpen are wireless communication modules, which support LTE-FDD, LTE-TDD, GSM/GPRS network data connection, they provide voice function for your special applications, and also support GNSS1). The following table shows the frequency bands of the modules.

Table 2: Frequency Bands of EC200U-CN QuecOpen Module

Network Mode	EC200U-CN QuecOpen
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
GSM	900 MHz/1800 MHz
GNSS[1)]	GPS, GLONASS, BeiDou, Galileo, QZSS
Bluetooth & Wi-Fi Scan[2)]	support

Table 2: Frequency Bands of EC200U-EU QuecOpen Module

Network Mode	EC200U-EU QuecOpen
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41
GSM	850 MHz/900 MHz/1800 MHz/1900 MHz
GNSS[1)]	GPS, GLONASS, BeiDou, Galileo, QZSS
Bluetooth & Wi-Fi Scan[2)]	support

With a compact profile of 28.0 mm × 31.0 mm × 2.4 mm, EC200U series QuecOpen can meet almost all requirements for M2 M applications such as automotive, metering, tracking system, security, router,

wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC200U series QuecOpen are SMD type modules which can be embedded into applications through 144-pin pads, including 80 LCC signal pads and 64 LGA pads.

NOTES

1. [1)] GNSS function is optional.
2. [2)] Bluetooth and Wi-Fi Scan functions cannot be used at the same time, you can only choose one.

2.2. Key Features

The following table describes the detailed features of EC200U series QuecOpen modules.

Table 3: Key Features of EC200U series QuecOpen Module

Feature	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 for GSM850 ● Class 4 for EGSM900 ● Class 1 for DCS1800 ● Class 1 for PCS1900 ● Class 3 for LTE-FDD bands ● Class 3 for LTE-TDD bands
LTE Features	● Support Cat 1 FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Support MIMO in DL direction ● FDD: Max 10 Mbps (DL), Max 5 Mbps (UL) ● TDD: Max 8.96 Mbps (DL), Max 3.1 Mbps (UL)
GSM Features	**GPRS:** ● Support GPRS multi-slot class 12 ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Max 85.6Kbps (DL)/Max 85.6Kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS protocols ● Support PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast

	● SMS storage
(U)SIM Interface	● Support USIM/SIM card: 1.8 V, 3.0 V
USB Interface	● Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade ● Support USB serial drivers for Windows 7/8/8.1/10, Linux 2.6/3.x/4.1~4.14, Android 4.x~9.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rates reach up to 921600 bps; 115200 bps by default ● Support MAIN_RTS and MAIN_CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 921600 bps baud rates ● Can only be used as a debugging serial port, not a general serial port **Auxiliary UART**
I2 C Interfaces	● Two I2 C signals
SPI Interface	● SPI interface only supports master mode
External Flash Interface	● Support external Flash chip
Audio Features	● Support one analog audio input and one analog audio output ● GSM:HR/FR/EFR/AMR/AMR-WB ● Support echo cancellation and noise suppression
LCD Interface	● LCD interface supporting SPI mode
Camera Interface	Support camera interface, I/O interface only supports 1.8 V, up to 300,000 pixel camera Support SPI serial 2-bit mode
Matrix keyboard interfaces	● Support 3 x 6 matrix keyboard [3)]
SD Card Interface	● Support SD 2.0 protocol
WLAN Interface*	● Support SDIO 1.1 interface for WLAN function
ADC Interfaces	● Provide three-way digital-to-analog conversion interface
USB_BOOT Interfaces	● Forced download interface
AT Commands	● Compliant with 3 GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indications	● Two pins including NET_MODE and NET_STATUS to indicate network

	connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Wi-Fi Scan/Bluetooth antenna interface (ANT_BT/WIFI_SCAN) ● GNSS antenna interface (ANT_GNSS)
Location	● Support Wi-Fi Scan/GNSS
Physical Characteristics	● Size: (28.0 ±0.15) mm × (31.0 ±0.15) mm × (2.4 ±0.2) mm ● Weight: approx. 4.1 g
Temperature Ranges	● Operation temperature range: -35 °C to +75 °C [1)] ● Extended temperature range: -40 °C to +85 °C [2)] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface and DFOTA
RoHS	● All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)]Within operation temperature range, the module is 3 GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operation temperature levels, the module will meet 3 GPP specifications again.
3. [3)]The GNSS function of the module is optional: if the selected module does not support the GNSS function, you can use the 3 x 6 matrix keyboard; If the selected module supports GNSS function, you can use 3 x 4 matrix keyboard.

2.3. Functional Diagram

The following figure shows a block diagram of EC200U series QuecOpen and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

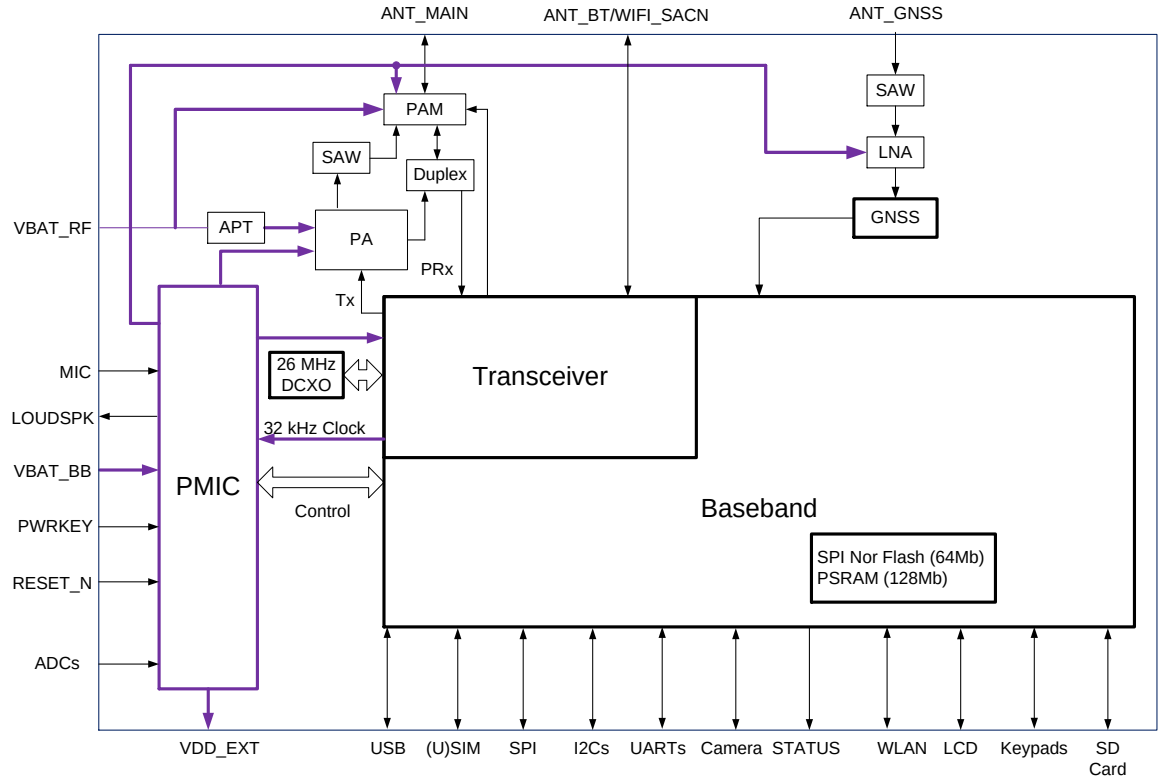


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications with EC200U series QuecOpen, Quectel provides an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antennas and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

EC200U series QuecOpen is equipped with 80 LCC pads plus 64 LGA pads that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI interface
- Analog audio interfaces
- LCD interface
- Camera interface
- Matrix keyboard interfaces
- SD card interface
- WLAN interface*
- ADC interfaces
- Status indications
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC200U series QuecOpen module.

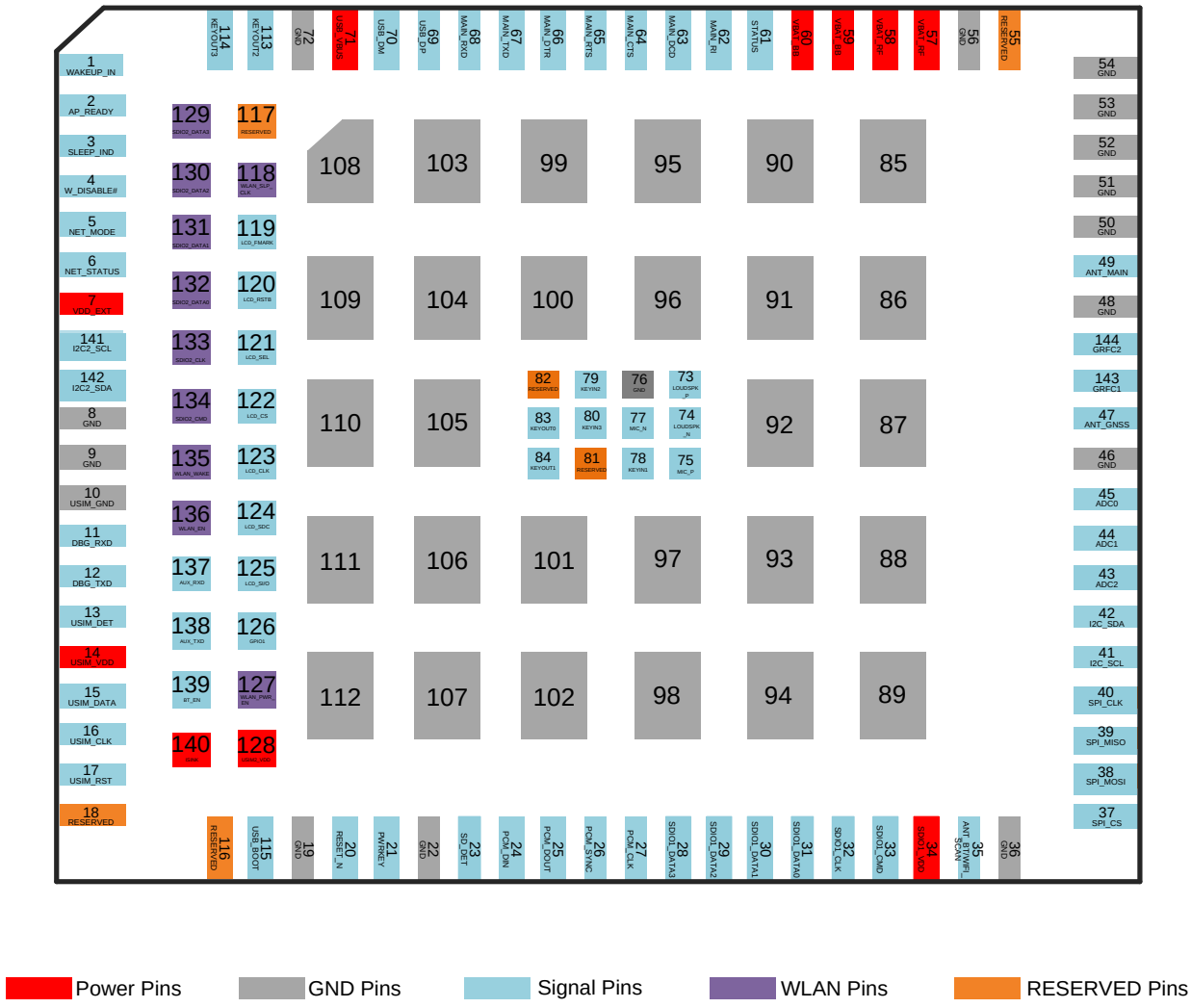


Figure 2: Pin Assignment (Top View)

NOTES

1. Pins USB_BOOT and KEYIN1 cannot be pulled up before startup.
2. Please keep all RESERVED and unused pins unconnected, and all GND pins are connected to the ground network.

3.3. Pin Description

The following tables show the pin definition of EC200U series QuecOpen module.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part and RF part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 1.5 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 2 A in a burst transmission.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112				
Module output power					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. When using, add 2.2 μF capacitor. If unused, keep it open.
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT voltage domain
RESET_N	20	DI	Reset the module	V_{IL}max = 0.5 V	VBAT voltage domain, If unused, keep it open. Active Low
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	DO	Indicate module's operating status		1.8 V power domain. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	Used for USB detection	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical: 5.0 V If unused, keep it open.
USB_DP	69	AIO	USB differential data bus (+)		Require differential impedance of 90 Ω. If unused, keep it open. USB 2.0 compliant.
USB_DM	70	AIO	USB differential data bus (-)		Require differential impedance of 90 Ω.

					If unused, keep it open. USB 2.0 compliant.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		(U)SIM card GND		GND connected to (U)SIM card connector.
USIM_VDD	14	PO	(U)SIM card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	17	DO	(U)SIM card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

USIM_DET	13	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	128	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_CTS	64	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.

Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	137	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
AUX_TXD	138	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC2	43	AI	General-purpose ADC interface	Voltage range: 0 V~VBAT_BB	Use 1 kΩ resistor in series; If unused, keep it open.
ADC1	44	AI	General-purpose ADC interface	Voltage range: 0 V~VBAT_BB	Use 1 kΩ resistor in series; If unused, keep it open.
ADC0	45	AI	General-purpose ADC interface	Voltage range: 0 V~VBAT_BB	Use 1 kΩ resistor in series; If unused, keep it open.
Analog audio interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LOUDSPK_P	73	AO	Loudspeaker differential output (+)		If unused, keep it open.

LOUDSPK_N	74	AO	Loudspeaker differential output (-)		If unused, keep it open.
MIC_P	75	AI	Microphone analog input (+)		If unused, keep it open.
MIC_N	77	AI	Microphone analog input (-)		If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		It needs to be pulled up to 1.8 V externally when in use; If unused, keep it open.
I2C_SDA	42	OD	I2C serial data		It needs to be pulled up to 1.8 V externally when in use; If unused, keep it open.
I2C2_SCL	141	OD	I2C serial clock		It needs to be pulled up to 1.8 V externally when in use; If unused, keep it open.
I2C2_SDA	142	OD	I2C serial data		It needs to be pulled up to 1.8 V externally when in use; If unused, keep it open.
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If you use a module model that supports GNSS function, the SPI function of pins 37–40 cannot be used and needs to be left unconnected..
SPI_MOSI	38	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_MISO	39	DI	SPI master mode input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_CLK	40	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

LCD Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_FMARK	119	DI	LCD frame synchronization	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
LCD_RSTB	120	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
LCD_SEL	121	DO	RESERVED		1.8 V power domain. If unused, keep it open.
LCD_CS	122	DO	LCD chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
LCD_CLK	123	DO	LCD clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
LCD_SDC	124	DO	LCD register selection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
LCD_SI/O	125	DIO	LCD data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
ISINK	140	PI	Sink current input pin, backlight adjustment	Imax = 200 mA Configurable current	Drive by sink current, connect to the cathode of the backlight, Adjust the brightness by adjusting the current.
Matrix keyboard interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
KEYIN1	78	DI	Matrix key input1		1.8 V power domain. If unused, keep it open. The KEYIN1 cannot be pulled up before startup.
KEYIN2	79	DI	Matrix key input2		1.8 V power domain. If unused, keep it open.
KEYIN3	80	DI	Matrix key input3		1.8 V power domain. If unused, keep it open.
KEYOUT0	83	DO	Matrix key output0		1.8 V power domain. If unused, keep it open.

KEYOUT1	84	DO	Matrix key output1		1.8 V power domain. If unused, keep it open.
KEYOUT2	113	DO	Matrix key output2		1.8 V power domain. If unused, keep it open.
KEYOUT3	114	DO	Matrix key output3		1.8 V power domain. If unused, keep it open.
KEYOUT4[1)]	81	DO	Matrix key output4		1.8 V power domain. If unused, keep it open.
KEYOUT5[2)]	82	DO	Matrix key output5		1.8 V power domain. If unused, keep it open.
SD Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	SD card detect		1.8/3.2 V If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA2	29	DIO	SDIO data bit 2		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA1	30	DIO	SDIO data bit 1		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA0	31	DIO	SDIO data bit 0		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_CLK	32	DO	SDIO clock		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_CMD	33	DIO	SDIO command		1.8/3.2 V power domain. If unused, keep it open.
SDIO1_VDD	34	PO	SDIO power supply		1.8/3.2 V power domain.

					If unused, keep it open.
WLAN Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDIO2_CLK	133	DO	WLAN SDIO CLK	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO2_CMD	134	DO	WLAN SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_WAKE	135	DI	Wake up the host by an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	

WLAN_EN	136	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Antenna interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_BT/WIFI_SCAN	35	AIO	Wi-Fi Scan/ Bluetooth antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	the module must enter the download mode to download; before turning on, pull this pin to a high level, and the module will enter the download mode.	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V voltage domain, high level is effective; a circuit design for entering download mode must be reserved.
OTHER Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
AP_READY	2	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SLEEP_IND	3	DO	Sleep indicator	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Flight mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	1.8 V power domain. Pull up by default. Driving the pin low can make the

				V_{IH}max = 2.0 V	module enter the flight mode.
RESERVED Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	18,55, 116,117,121				Keep these pins open.

NOTE

The GNSS function of the module is optional: if the selected module does not support the GNSS function, you can use the 3 x 6 matrix keyboard; If the selected module supports GNSS function, you can use 3 x 4 matrix keyboard.

3.4. Specific multiplexing interface function description

Table 5: External Flash and camera interface multiplexing function description

External Flash interface multiplexing mode (multiplex dedicated interface connects to Flash)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	27	DO	SPI_FLASH1_CLK	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to the clock of the external Flash chip
PCM_SYNC	26	DO	SPI_FLASH1_CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Chip select for external Flash chip
PCM_DIN	24	IO	SPI_FLASH1_SIO_0	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to IO0 of external Flash chip
PCM_DOUT	25	IO	SPI_FLASH1_SIO_1		Connect to IO1 of external Flash chip
USIM_DET	13	IO	SPI_FLASH1_SIO_2		Connect to IO2 of external Flash chip
WLAN_WAKE	135	IO	SPI_FLASH1_SIO_3		Connect to IO3 of external Flash chip
CAMERA Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	CAM_SCK		Camera SPI mode clock input signal, 1.8 V power domain.

STATUS	61	DO	CAM_RST	Low-end cameras are generally not used, 1.8 V power domain.
MAIN_RI	62	DO	CAM_PWDN	Camera power down control, 1.8 V power domain.
MAIN_DCD	63	DO	CAM_REFCLK	Camera master clock output signal，1.8 V power domain.
MAIN_DTR	66	IO	CAM_DATA0	Camera SPI data 0，1.8 V power domain.
NET_STATUS	6	IO	CAM_DATA1	Camera SPI data 1，1.8 V power domain.

3.5. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN = 0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN = 4** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit (PMU) shuts down the power supply. Software is not active, the serial interface is not accessible, while operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.6. Power Saving

3.6.1. Sleep Mode

EC200U series QuecOpen is able to reduce its current consumption to a minimum value in sleep mode. The following section describes power saving procedures of EC200U series QuecOpen module.

3.6.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK = 1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

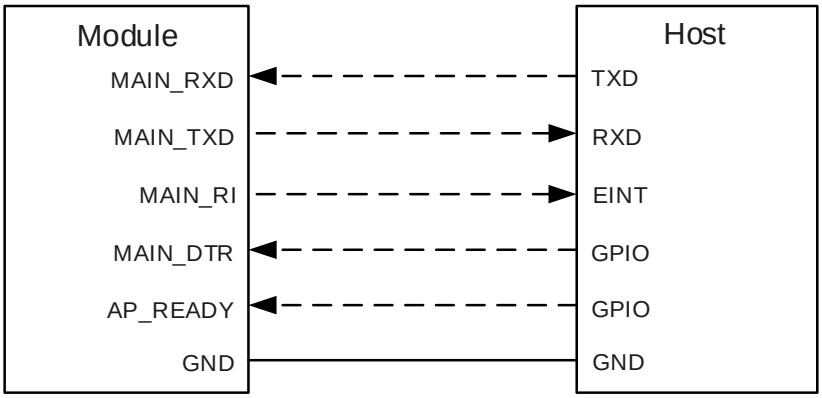


Figure 3: Sleep Mode Application via UART

- The host drives MAIN_DTR to low level will wake up the module.
- When EC200U series QuecOpen has a URC to report, MAIN_RI signal will act. Please refer to ***Chapter 3.24*** for details about **MAIN_RI** behavior.

3.6.1.2. USB Application with USB Remote Wakeup Function*

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK = 1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

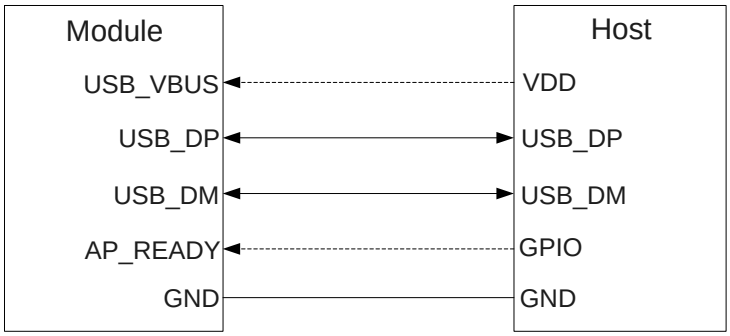


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC200U series QuecOpen through USB will wake up the module.
- When EC200U series QuecOpen has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

NOTE

Under Linux system, USB can be suspended while under Windows system, it cannot be suspended.

3.6.1.3. USB Application with USB Suspend/Resume and MAIN_RI Function*

If the host supports USB suspend/resume however does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK = 1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

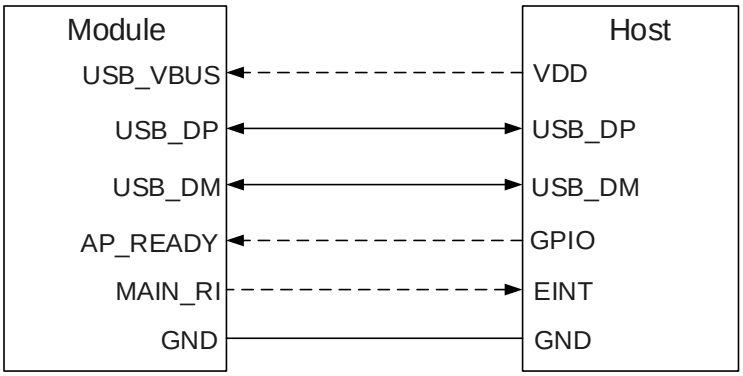


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to module through USB will wake up the module.
- When the module has a URC to report, RI signal wakes up the host.

NOTE

Under Linux system, USB can be suspended while under Windows system, it cannot be suspended.

3.6.1.4. USB Application

If the host does not support USB suspend function, USB_VBUS should be disconnected via additional control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK = 1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

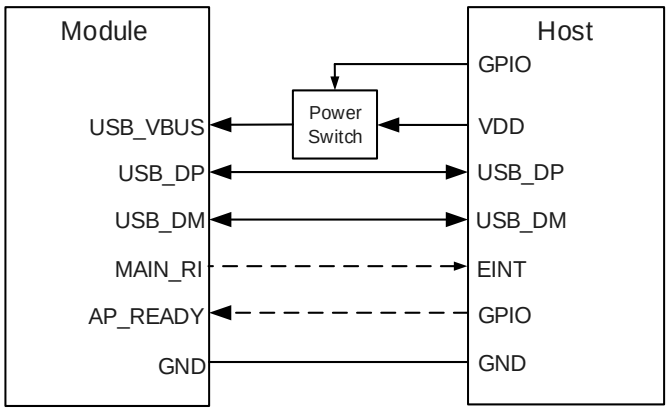


Figure 6: Sleep Mode Application without Suspend Function

The module will be waken up when switching on the power switch to supply power to USB_VBUS.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.6.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG = "airplanecontrol",1** can be used to enable the function. Driving it to low level can make the module enter airplane mode.

Software:

AT+CFUN command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN = 0:** Minimum functionality mode;(RF functions are disabled).
- **AT+CFUN = 1:** Full functionality mode (by default).
- **AT+CFUN = 4:** RF function is disabled(Airplane mode).

NOTE

"*" means it is under development.

3.7. Power Supply

3.7.1. Power Supply Pins

EC200U series QuecOpen provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part and RF part.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part and RF part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72,76, 85~112	Ground	-	0	-	V

3.7.2. Decrease Voltage Drop

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2 G network. The voltage drop will be less in 3 G and 4 G networks.

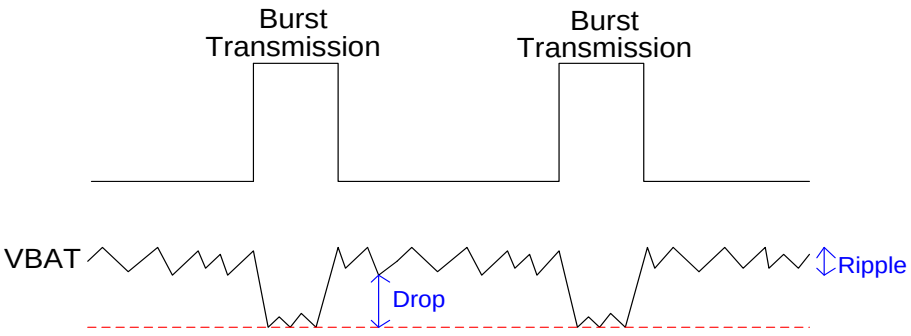


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB and VBAT_RF. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 2 mm; and the width of VBAT_RF trace should be no less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 Watts should be used. The following figure shows the star structure of the power supply.

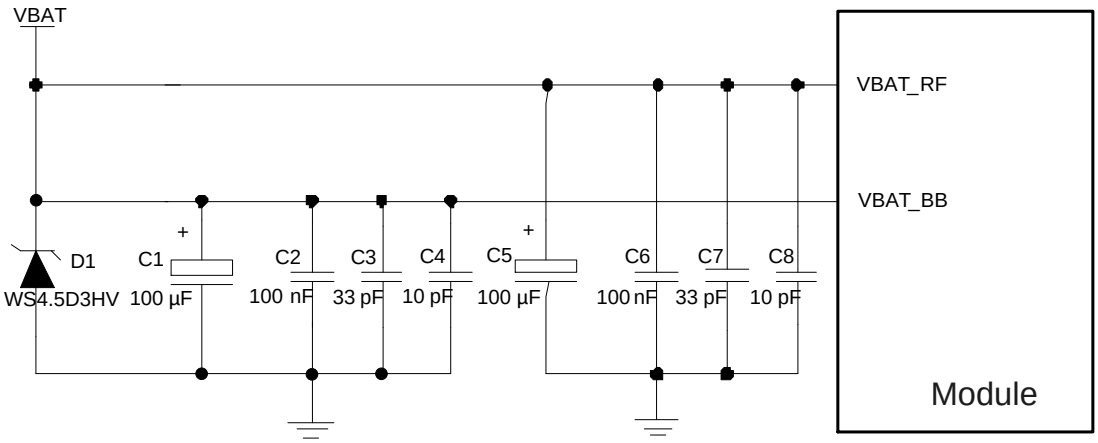


Figure 8: Star Structure of Power Supply

3.7.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A at least to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

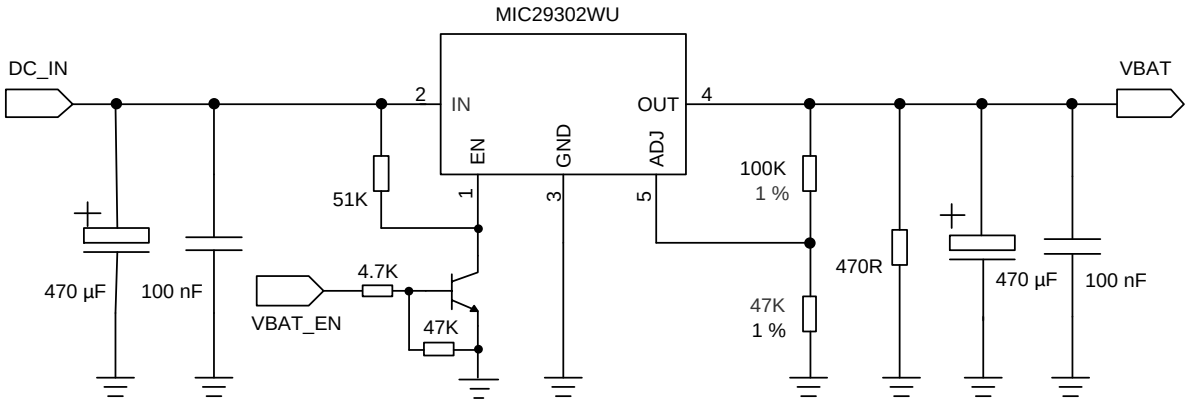


Figure 9: Reference Circuit of Power Supply

3.8. Power-on/off Scenarios

3.8.1. Turn on Module Using the PWRKEY

Table 8: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT voltage domain

When EC200U series QuecOpen is in power down mode, it can be turned on to normal mode by driving PWRKEY pin to a low level for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

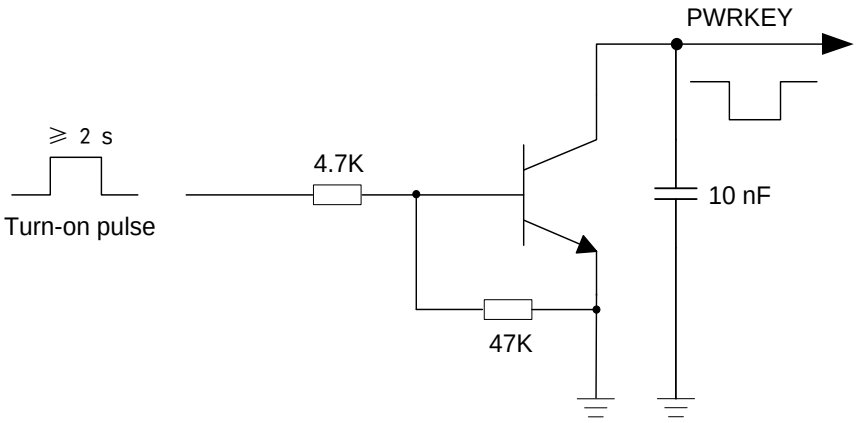


Figure 10: Turn on Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the key for ESD protection.

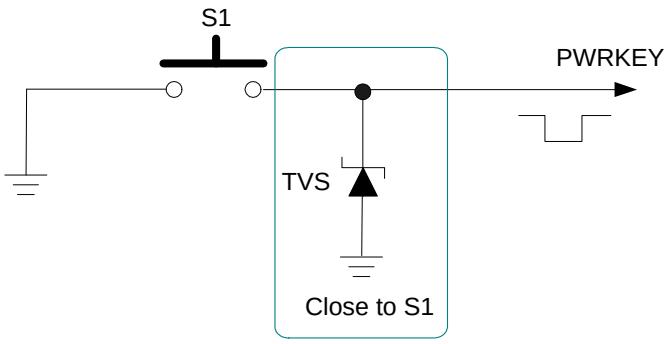


Figure 11: Turn on Module through Keystroke

The timing of turning on the module is illustrated in the following figure.

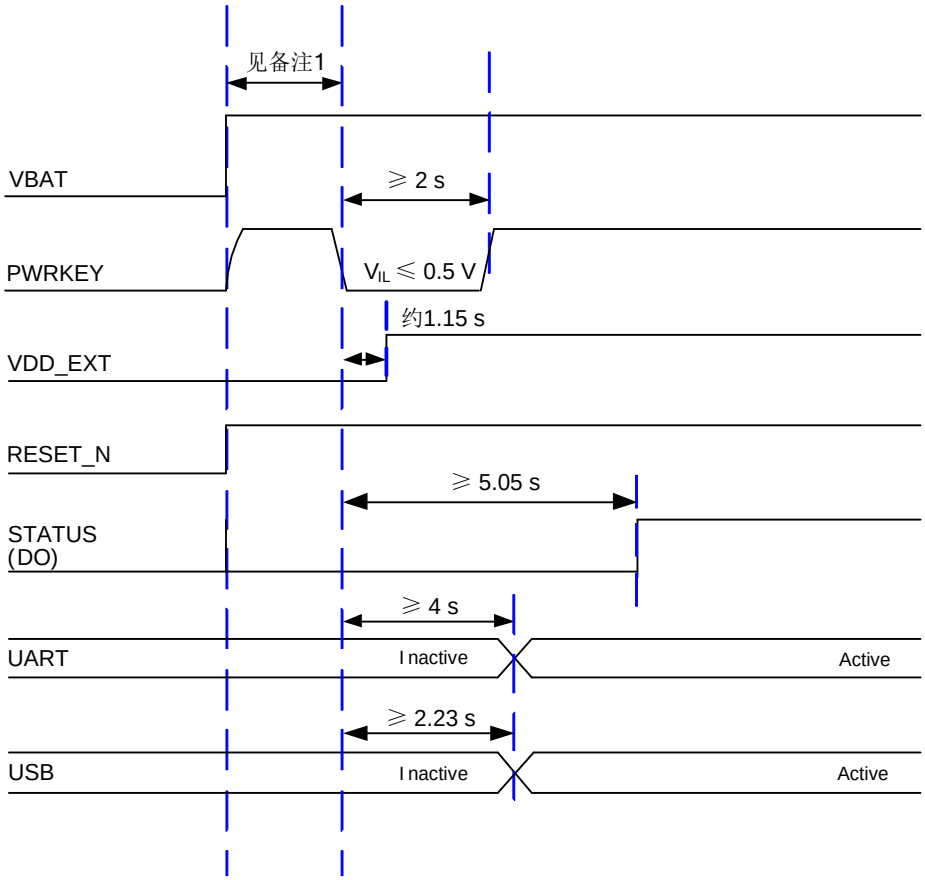


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1K resistor if module needs to be powered on automatically and shutdown is not needed.

3.8.2. Turn off Module

The following procedures can be used to turn off the module:

- Turn off the module using PWRKEY pin.
- Turn off the module using **AT+QPOWD** command.

3.8.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 3 S, the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

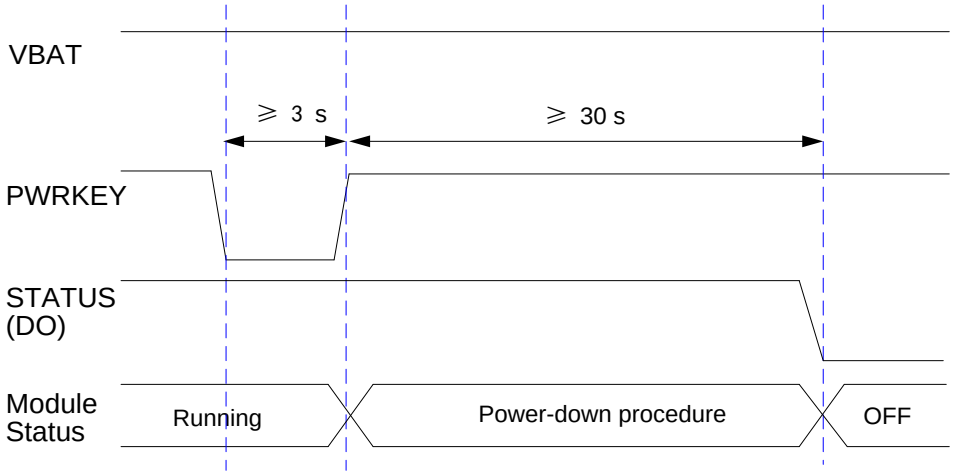


Figure 13: Timing of Turning off Module

3.8.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When keeping the PWRKEY to the ground and the AT command cannot be used to turn off, the module can only be forced to turn off by cutting off the VBAT power supply. Therefore, we recommend that you can turn on or turn off the module by pulling up and pulling down the PWEKEY instead of keeping the PWRKEY to the ground.

3.9. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 9: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

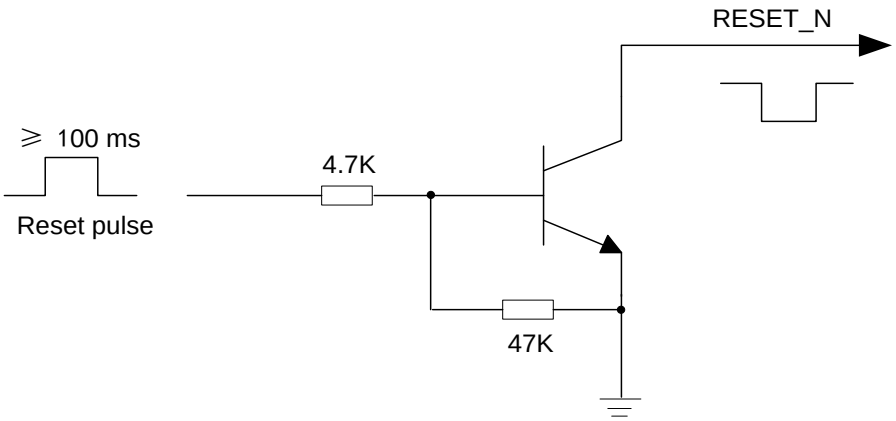


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

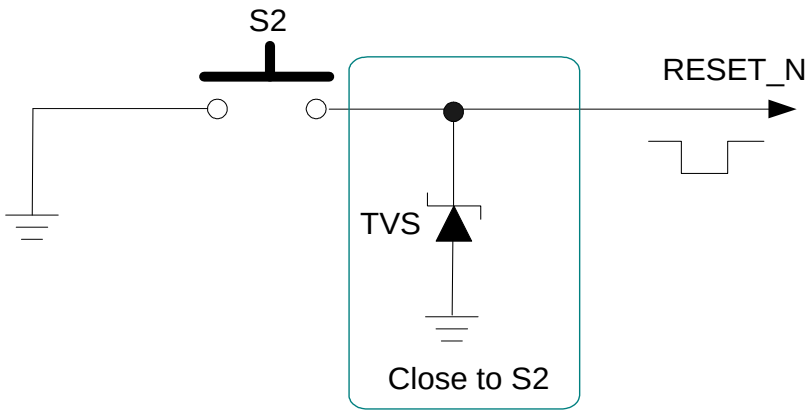


Figure 15: Reference Circuit of RESET_N by Using Button

The timing of resetting module is illustrated in the following figure.

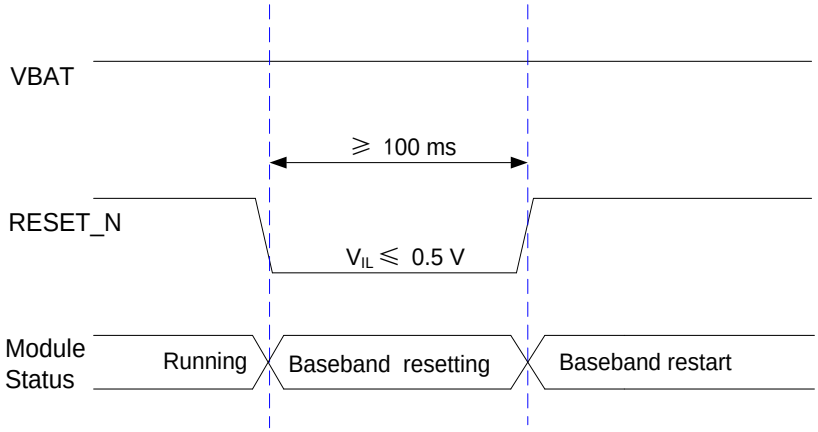


Figure 16: Timing of Resetting Module

NOTES

1. Ensure that there is no large capacitance on PWRKEY and RESET_N pins, and the maximum is not more than 10 nF.
2. It is recommended to use RESET_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

3.10. (U)SIM Interface

EC200U series QuecOpen module provides a (U)SIM interface.The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	IO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	

USIM_DET	13	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_GND	10		Specified ground for (U)SIM card	

EC200U series QuecOpen supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low level and high level detections. By default, it is disabled, and can be opened by software configuration. Please see ***document [2]*** for more details about the **AT+QSIMDET** command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

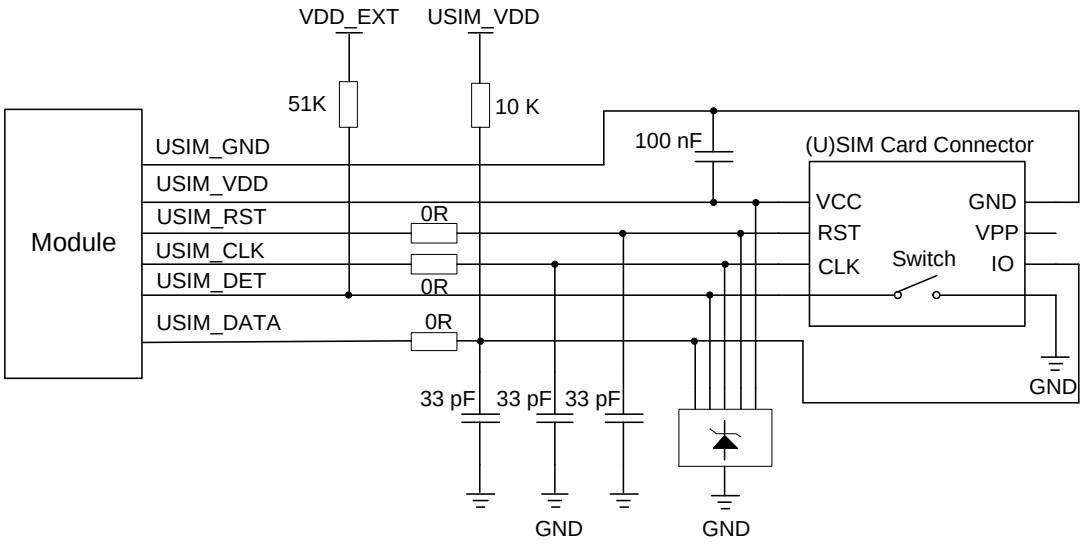


Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

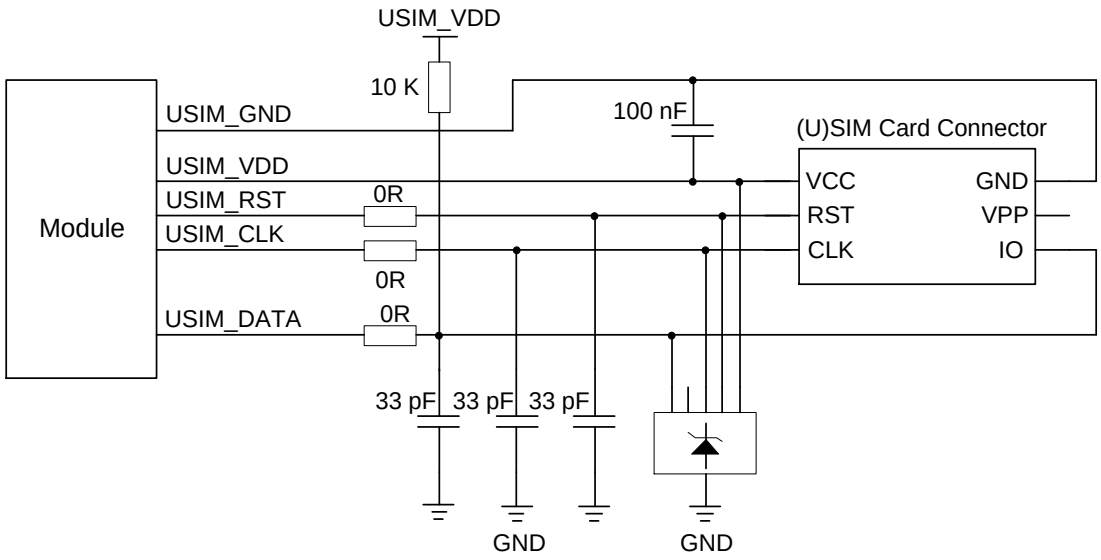


Figure 18: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability upon applying of long layout trace and sensitive occasion, and should be placed close to the (U)SIM card connector.

3.11. USB Interface

EC200U series QuecOpen contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface only supports USB slave mode.This interface is used for AT command communication, data transmission, software debugging, firmware upgrade and voice over USB. The following table shows

the pin definition of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB differential data bus (+)	Require differential impedance of 90 Ω
USB_DM	70	AIO	USB differential data bus (-)	Require differential impedance of 90 Ω
USB_VBUS	71	AI	USB connection detect	Typical 5.0 V, Minimum 3.5 V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

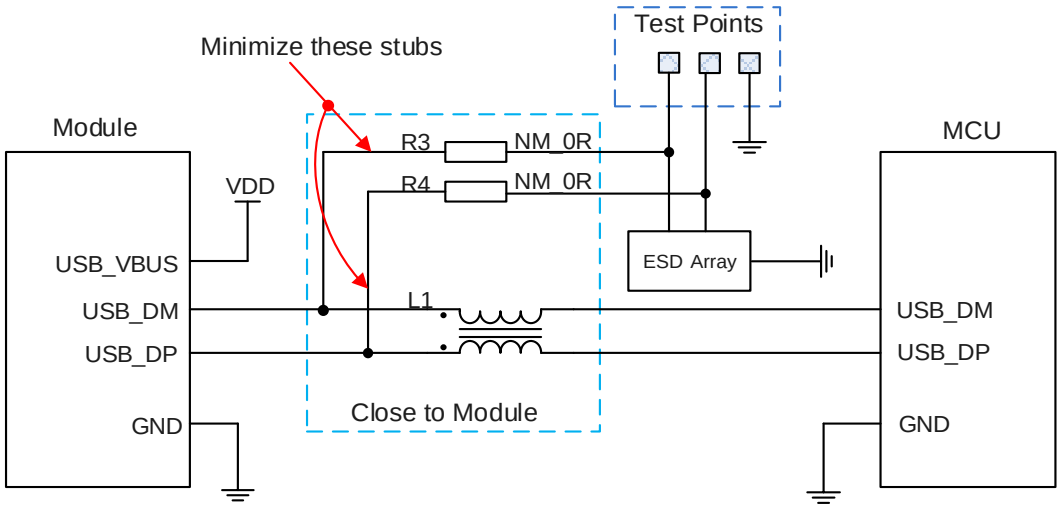


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2.0 pF,and keep the ESD protection components to the USB connector as close as possible.

3.12. UART Interfaces

The module provides three UART interfaces: the main UART interface 、the debug UART interface、auxiliary UART Interface. The following shows their features.

- Main UART interface ：The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication.
- Debug UART interface ：Only supports 921600 bps baud rate, it is used for the output of partial logs.
- Auxiliary UART Interface.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	Main UART clear to send	
MAIN_RTS	65	DI	Main UART request to send	
MAIN_DTR	66	DI	Main UART data terminal ready	
MAIN_TXD	67	DO	Main UART transmit	
MAIN_RXD	68	DI	Main UART receive	

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment

DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain. If unused, keep it open.
DBG_RXD	11	DI	Debug UART receive	

Table 13: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	138	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep it open.
AUX_RXD	137	DI	Auxiliary UART receive	

The module provides 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

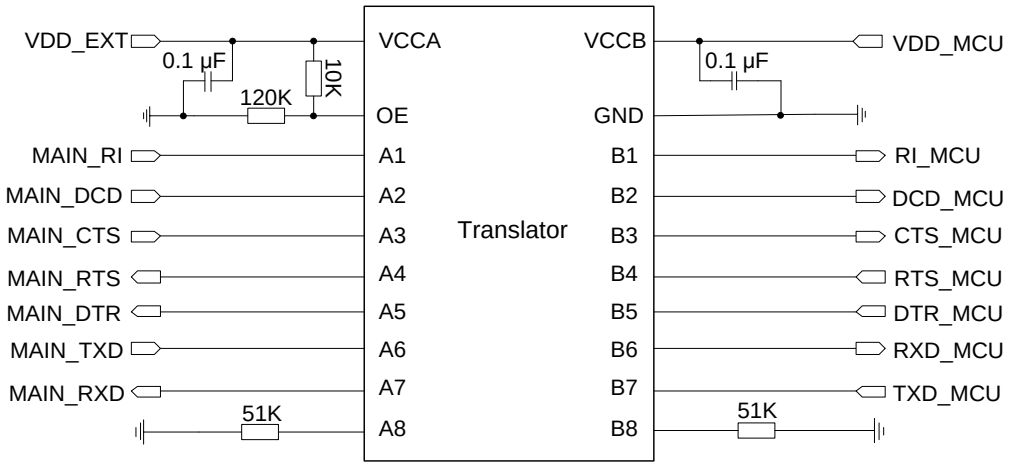


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For circuit design of dotted line section, the design of solid line section can server as reference in terms of both module input and output circuit designs; but please pay attention to the direction of connection.

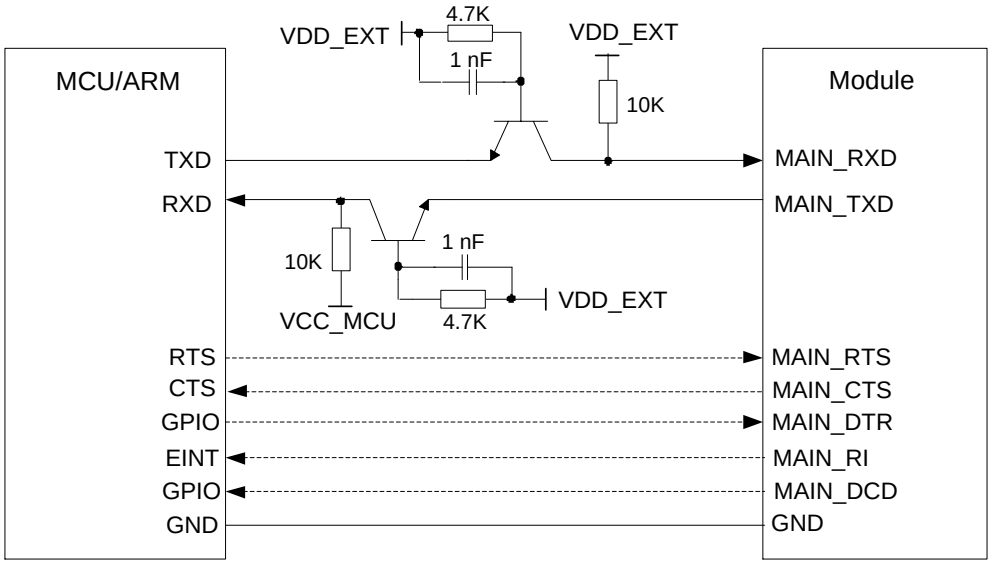


Figure 21: Reference Circuit with Transistor Circuit

NOTE

1. Triode level transistor circuit solution is not suitable for applications with baud rates exceeding 460Kbps.
2. Please note that the CTS and RTS pins of the serial port hardware flow control are directly connected, and pay attention to the input and output directions.

3.13. I2C Interfaces

EC200U series QuecOpen provides two I2C interface.

Table 14: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8 V. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	Require external pull-up to 1.8 V. If unused, keep it open.
I2C2_SCL	141	OD	I2C serial clock	Require external pull-up to 1.8 V. If unused, keep it open.
I2C2_SDA	142	OD	I2C serial data	Require external pull-up to 1.8 V. If unused, keep it open.

3.14. SPI Interface

The SPI interface of EC200U series QuecOpen module only supports master mode. It communicates between module and peripherals through synchronous full duplex. Its working voltage is 1.8 V, and the maximum clock rate is 30 MHz.

Table 15: SPI interface pin definition

SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If you use a module model that supports GNSS function, the SPI function of pins 37~40 cannot be used and needs to be left floating.
SPI_MOSI	38	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_MISO	39	DI	SPI master mode input		
SPI_CLK	40	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

3.15. External Flash interface

EC200U series QuecOpen module supports an external Flash chip, and the external Flash interface is multiplexed with other pin functions of the module. For details, please refer to the following methods:

Table 18: External Flash multiplexing function description

External Flash interface multiplexing mode (multiplex dedicated interface connects to Flash)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	27	DO	SPI_FLASH1_CLK	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to the clock of the external Flash chip
PCM_SYNC	26	DO	SPI_FLASH1_CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Chip select for external Flash chip
PCM_DIN	24	IO	SPI_FLASH1_SIO_0	V_{IL}min = -0.3 V	Connect to IO0 of external Flash chip

PCM_DOUT	25	IO	SPI_FLASH1_SIO_1	V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to IO1 of external Flash chip
USIM_DET	13	IO	SPI_FLASH1_SIO_2		Connect to IO2 of external Flash chip
WLAN_WAKE	135	IO	SPI_FLASH1_SIO_3		Connect to IO3 of external Flash chip

3.16. Analog audio interface

EC200U series QuecOpen module provides one analog audio input channel and one analog audio output channel. The pin definition is shown in the table below.

Table 19: Pin definition of analog audio interface

interface	Pin Name	Pin No.	I/O	Description
AOUT	LOUDSPK_P	73	AO	Loudspeaker differential output (+)
	LOUDSPK_N	74	AO	Loudspeaker differential output (-)
AIN	MIC_P	75	AI	Microphone analog input (+)
	MIC_N	77	AI	Microphone analog input (-)

- AIN channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- The AOUT channel is a differential output with a built-in power amplifier. When configured as AB power amplifier, the maximum driving power is 500 mW for 8 Ω load; when configured as D, the maximum driving power is 800 mW for 8 Ω load.

3.16.1. Notes on audio interface design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.16.2. Microphone interface circuit

The reference circuit of the microphone interface is shown in the figure below:

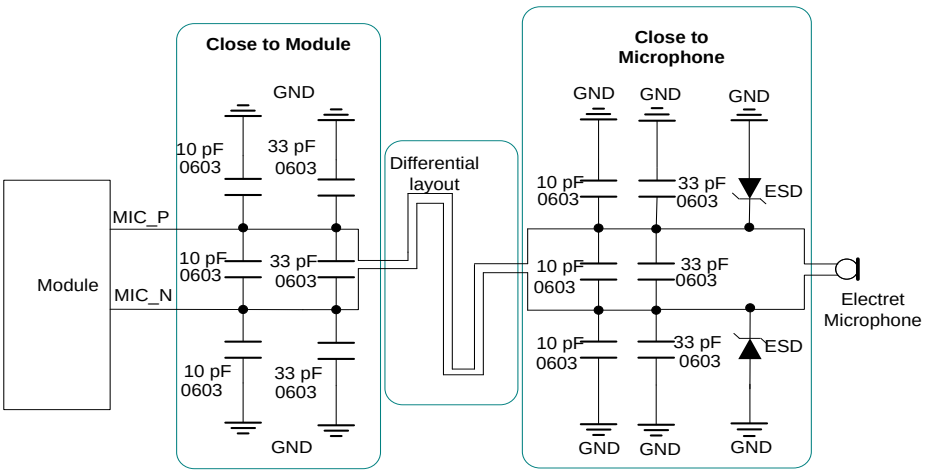


Figure 22:The reference circuit of the microphone interface

NOTE

Since the microphone channel is more sensitive to ESD, it is recommended not to omit the ESD protection device of the microphone channel.

3.16.3. Handset interface circuit

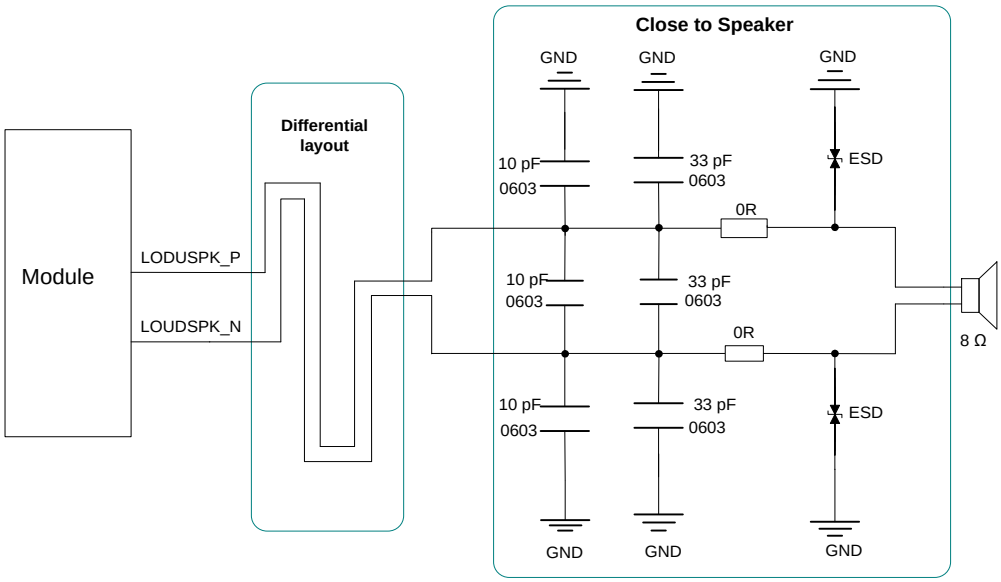


Figure 23:The reference circuit of the Handset interface

3.17. LCD Interface

The LCD interface of the module supports a liquid crystal display with a maximum resolution of 320 × 240; it supports DMA transmission, 16-bit RGB565 and YUV formats.

Pin Name	Pin No.	I/O	Description	Comment
LCD_FMARK	119	DI	LCD frame synchronization	1.8 V power domain. If unused, keep it open.
LCD_RSTB	120	DO	LCD reset	1.8 V power domain. If unused, keep it open.
LCD_SEL	121	DO	RESERVED	1.8 V power domain. If unused, keep it open.
LCD_CS	122	DO	LCD chip select	1.8 V power domain. If unused, keep it open.
LCD_CLK	123	DO	LCD clock	1.8 V power domain. If unused, keep it open.
LCD_SDC	124	DO	LCD register selection	1.8 V power domain. If unused, keep it open.
LCD_SI/O	125	I/O	LCD data	1.8 V power domain. If unused, keep it open.
ISINK	140	PI	Sink current input pin, backlight adjustment	Imax = 200 mA .Drive by sink current, connect to the cathode of the backlight, through

				adjustment Electric current to adjust the brightness.

3.18. Camera Interface

EC200U series QuecOpen module supports camera interface. The camera interface is multiplexed with other pin functions. The I/O interface only supports 1.8 V, can support up to 300,000 pixels of cameras, and supports SPI serial 2-bit mode.

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	CAM_SCK	Camera SPI mode clock input signal, 1.8 V power domain.
STATUS	61	DO	CAM_RST	Low-end cameras are generally not used, 1.8 V power domain.
MAIN_RI	62	DO	CAM_PWDN	Camera power down control, 1.8 V power domain.
MAIN_DCD	63	DO	CAM_REFCLK	Camera master clock output signal，1.8 V power domain.
MAIN_DTR	66	IO	CAM_DATA0	Camera SPI data 0，1.8 V power domain.
NET_STATUS	6	IO	CAM_DATA1	Camera SPI data 1，1.8 V power domain.
I2C_SCL	41	OD		The camera I2C serial clock needs to be pulled up externally to VDD_EXT. 1.8 V power domain. If unused, keep it open.
I2C_SDA	42	OD		The camera I2C serial data needs to be pulled up externally to VDD_EXT. 1.8 V power domain. If unused, keep it open.

3.19. Matrix keyboard interface

EC200U series QuecOpen module provides button interface. The GNSS function of the module is optional: if the selected module does not support the GNSS function, you can use the 3 x 6 matrix keyboard; If the selected module supports GNSS function, you can use 3 x 4 matrix keyboard.

Matrix keyboard interface pin definition：

Pin Name	Pin No.	I/O	Description	Comment
KEYIN1	78	DI	Matrix key input1	1.8 V power domain. If unused, keep it open. The KEYIN1 cannot be pulled up

				before startup.
KEYIN2	79	DI	Matrix key input2	1.8 V power domain. If unused, keep it open.
KEYIN3	80	DI	Matrix key input3	1.8 V power domain. If unused, keep it open.
KEYOUT0	83	DO	Matrix key output0	1.8 V power domain. If unused, keep it open.
KEYOUT1	84	DO	Matrix key output1	1.8 V power domain. If unused, keep it open.
KEYOUT2	113	DO	Matrix key output2	1.8 V power domain. If unused, keep it open.
KEYOUT3	114	DO	Matrix key output3	1.8 V power domain. If unused, keep it open.
KEYOUT4[1)]	81	DO	Matrix key output4	1.8 V power domain. If unused, keep it open.
KEYOUT5[2)]	82	DO	Matrix key output5	1.8 V power domain. If unused, keep it open.

NOTE

The GNSS function of the module is optional: if the selected module does not support the GNSS function, you can use the 3 x 6 matrix keyboard; If the selected module supports GNSS function, you can use 3 x 4 matrix keyboard.

3.20. SD Card Interface

EC200U series QuecOpen supports SDIO 3.0 interface for SD card.

Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	SD card detect	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA2	29	DIO	SDIO data bit 2	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA1	30	DIO	SDIO data bit 1	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_DATA0	31	DIO	SDIO data bit 0	1.8/3.2 V power domain. If unused, keep it open.

SDIO1_CLK	32	DO	SDIO clock	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_CMD	33	DIO	SDIO command	1.8/3.2 V power domain. If unused, keep it open.
SDIO1_VDD	34	PO	SDIO power supply	1.8/3.2 V power domain. If unused, keep it open.

The following figure shows a reference design of SD card interface.

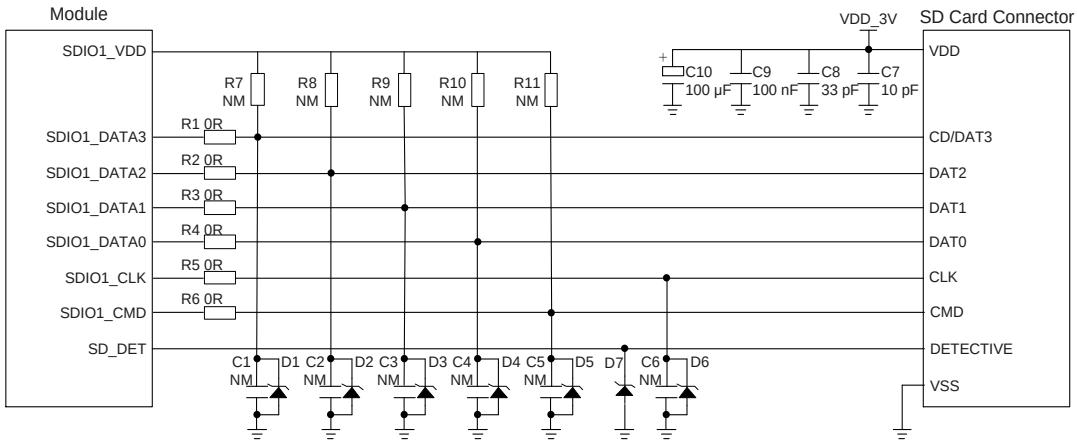


Figure 22: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3 V is 2.7 V~3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of VDD_SDIO is 150 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10KΩ~100KΩ and the recommended value is 100KΩ. VDD_SDIO1 should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω±10%.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDIO1_CLK and SDIO1_DATA[0:3]/

SDIO1_CMD less than 1 mm and the total routing length less than 50 mm.

3.21. WLAN Interface*

EC200U series QuecOpen module provides a SDIO 1.1 standard WLAN interface.

Table 17: Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	1.8 V power domain. If unused, keep it open.
SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2	
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1	
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0	
SDIO2_CLK	133	DO	WLAN SDIO clock	
SDIO2_CMD	134	DO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the module	Wake up the host (module) through the external Wi-Fi module. 1.8 V power domain. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control	1.8 V power domain. If unused, keep it open.

The SDIO interface rate is very high. To ensure that the interface design complies with the SDIO 1.1 specification, the following principles are recommended:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω±10%.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between WLAN_SDIO_CLK and WLAN_SDIO_DATA[0:3]/ WLAN_SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.

NOTE

If the WLAN control interface conflicts with other functions, please consult technical supports of Quectel.

3.22. ADC Interfaces

The module provides three analog-to-digital converter (ADC) interfaces. **AT+QADC = 0** can be used to read the voltage value on ADC0 pin. **AT+QADC = 1** can be used to read the voltage value on ADC1 pin. **AT+QADC = 2** can be used to read the voltage value on ADC2 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 18: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC0	45	General-purpose ADC interface	Use a 1 kΩ resistor in series; if unused, keep it open.
ADC1	44	General-purpose ADC interface	Use a 1 kΩ resistor in series; if unused, keep it open.
ADC2	43	General-purpose ADC interface	Use a 1 kΩ resistor in series; if unused, keep it open.

Table 19: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

3.23. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins for network status indication, which are NET_MODE and NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 20: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network registration mode	1.8 V power domain. If unused, keep it open.

Table 21: Working State of Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Always high	Registered on LTE network
	Always low	Others
NET_MODE	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Idle
	Flicker repeatly (62 s high/63 s low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

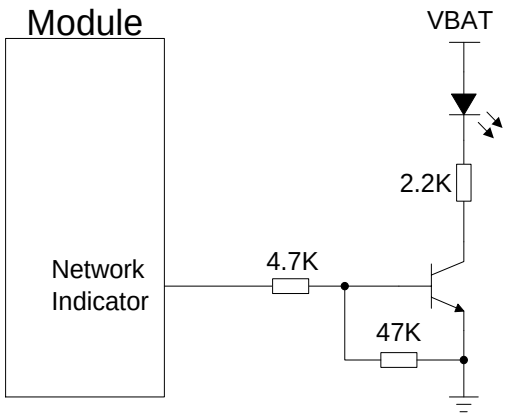


Figure 23: Reference Circuit of Network Indicator

3.24. STATUS

The STATUS pin is an open drain output for module's operation status indication. When the module is turned on normally, the STATUS will present the high state.

Table 22: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

The following figure shows different circuit designs of STATUS.

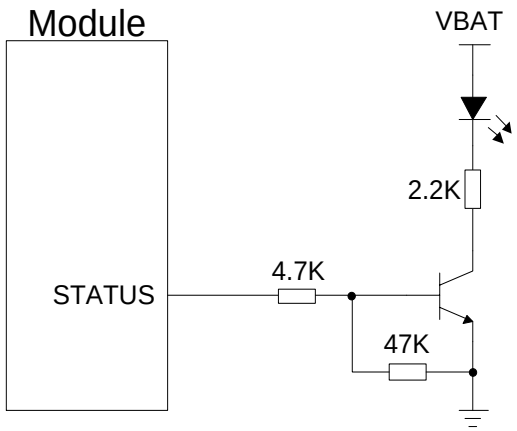


Figure 24: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT is removed.

3.25. Behaviors of the MAIN_RI

AT+QCFG = "risignaltype","physical" can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behaviors can be configured flexibly. The default behaviors of the MAIN_RI is shown as below.

Table 23: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be configured by **AT+QCFG = "urc/MAIN_RI/ring"**. Please refer to ***document [2]*** for details.

3.26. USB_BOOT Interface

EC200U series QuecOpen module needs to enter download mode to download. Customers can pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 24: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module into emergency download mode	1.8 V power domain. Active high. The download control circuit must be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

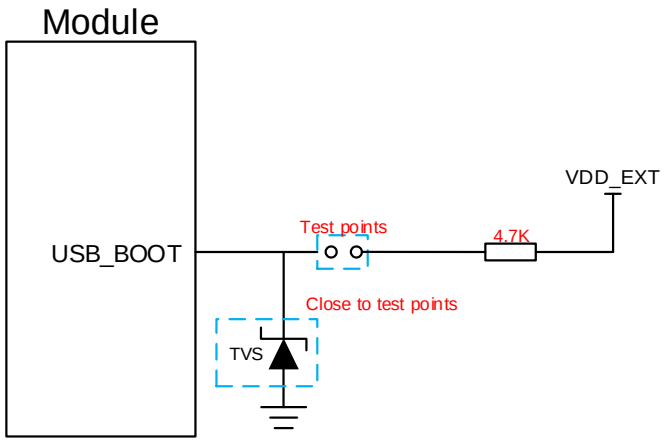


Figure 25: Reference Circuit of USB_BOOT Interface

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.

4 Antenna Interfaces

EC200U-CN antenna interfaces include a main antenna interface, a WiFi Scan&BT shared antenna interfaces which is used to resist the fall of signals caused by high speed movement and multipath effect. The antenna ports have an impedance of 50 Ω.

4.1. Main/BT Antenna Interfaces

4.1.1. Pin Definition

The pin definition of main antenna and WiFi Scan&BT shared antenna interfaces is shown below.

Table 25: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna interface	50 Ω impedance.
ANT_BT/WIFI_SCAN	35	AI	Wi-Fi Scan/Bluetooth antenna interface	50 Ω impedance. If unused, keep it open.

4.1.2. Operating Frequency

Table 26: EC200U-CN Operating Frequencies

3 GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	880~915	925~960	MHz

LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2535~2675	2535~2675	MHz

Table 27: EC200U-EU Operating Frequencies

3 GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-TDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B20	832–862	791–821	MHz
LTE-TDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and WiFiScan& Bluetooth antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

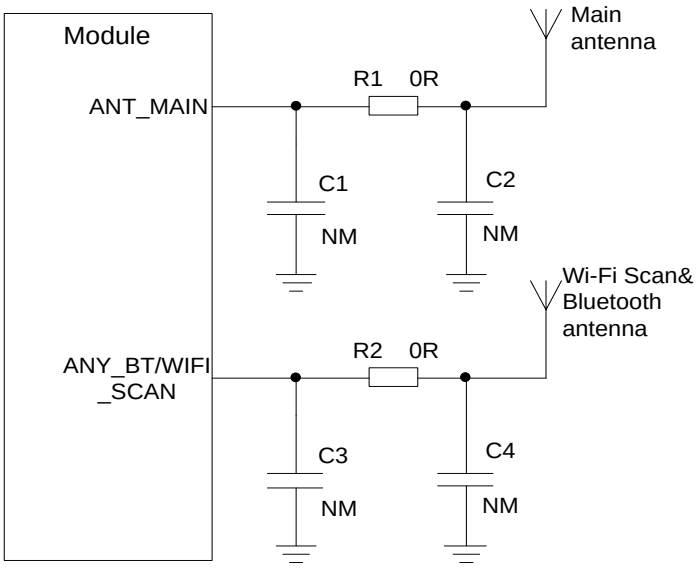


Figure 26: Reference Circuit of RF Antenna Interface

NOTES

1. In order to improve the receiving sensitivity, it is necessary to ensure the proper distance between the main antenna and the Bluetooth receiving antenna.
2. Place the π-type matching components (R1&C1&C2 and R2&C3&C4) as close to the antenna as possible.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

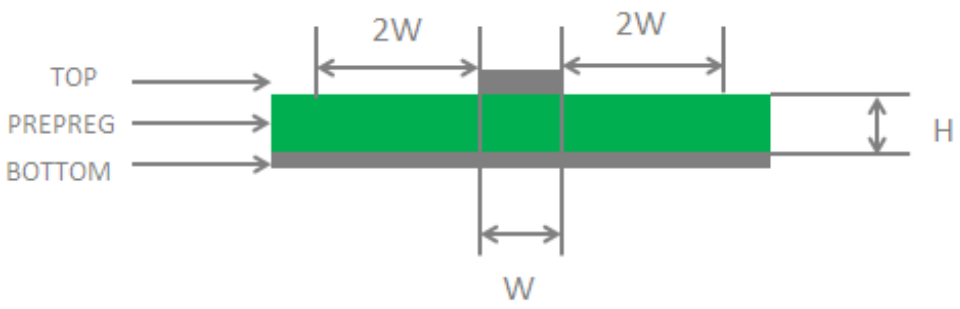


Figure 27: Microstrip Design on a 2-layer PCB

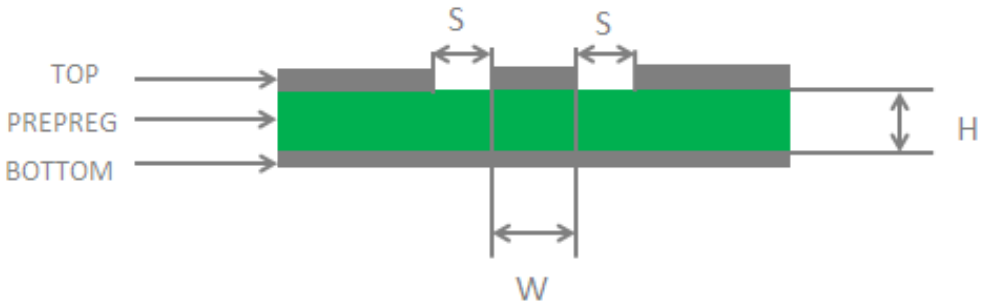


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

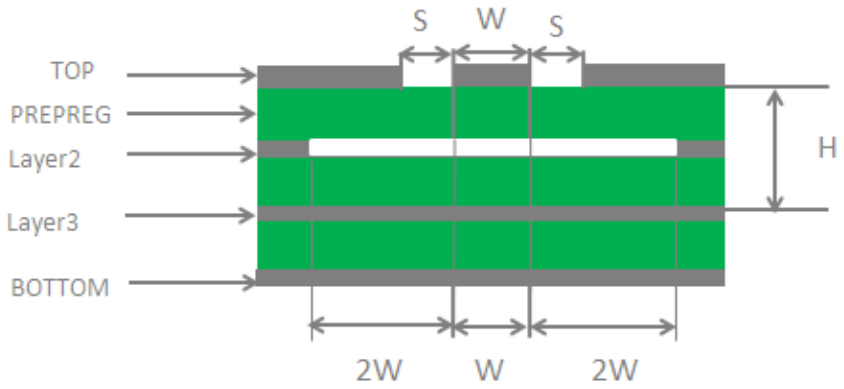


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

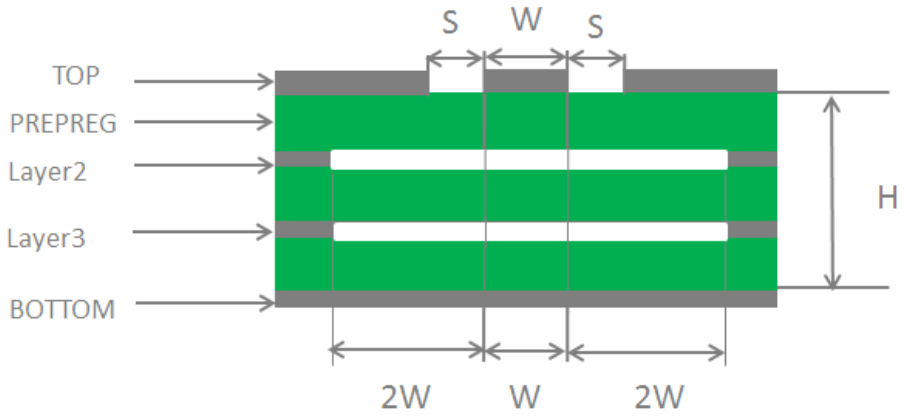


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

4.2. GNSS Antenna Interface

The following table lists the pin definitions and frequency characteristics of the GNSS antenna interface, respectively.

Table 28: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna pad	50 Ω impedance. If unused, keep it open.

Table 29: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou（Compass）	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below:

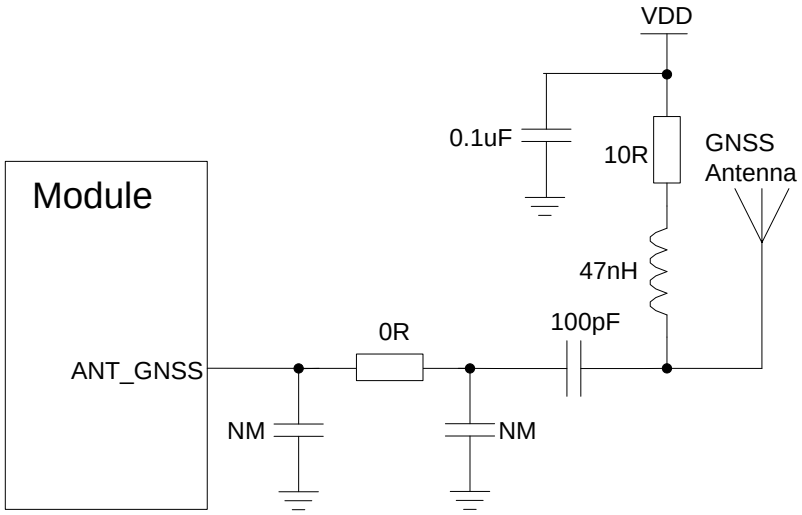


Figure 31: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

4.3. Antenna Installation

4.3.1. Antenna Requirement

The following table shows the requirements on main antenna.

Table 30: Antenna Requirements

Type	Requirements
GNSS	Frequency range 1: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (typ.) Passive antenna gain: > 0 dBi Active antenna noise factor: < 1.5 dB Active antenna gain: > 0 dBi Active antenna internal LNA gain: < 17 dB
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 %

	Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (GSM850/EGSM900, LTE-FDD B5/B8/B20/B28) Cable insertion loss: < 1.5 dB (DCS1800/PCS1900, LTE-FDD B1/B3) Cable insertion loss: < 2 dB (LTE-TDD B7/B34/B38/B39/B40/B41)

4.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

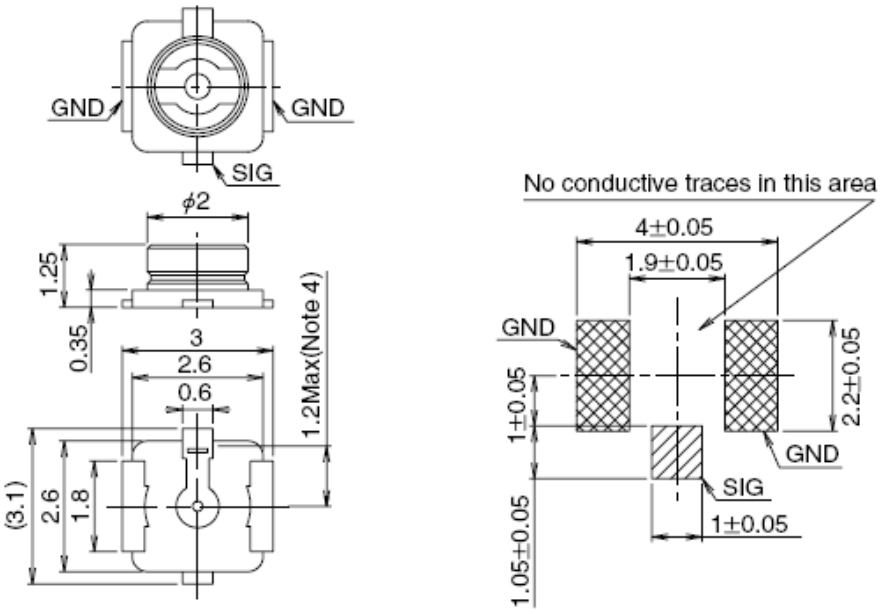


Figure 32: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

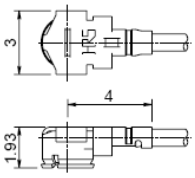
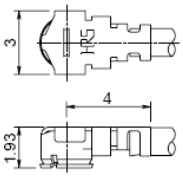
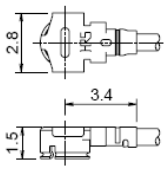
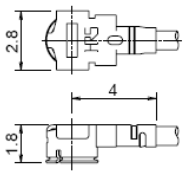
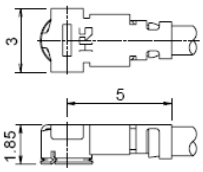
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 33: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

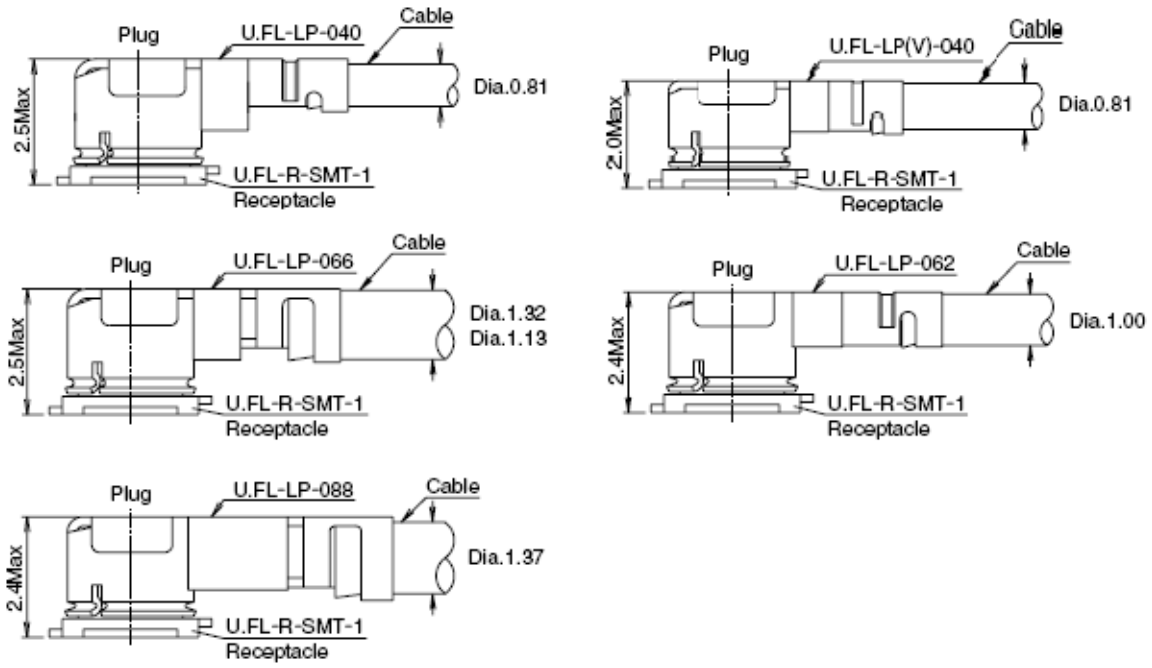


Figure 34: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1.5	A
Peak Current of VBAT_RF	0	2.0	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V
Voltage at ADC2	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 32: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit

VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB power supply; used for USB detection		3.5	5.0	5.25	V

5.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 33: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3 GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call*, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operation temperature levels, the module will meet 3 GPP specifications again.

5.4. Current Consumption

Table 34: EC200U-CN QuecOpen Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	μA
	AT+CFUN = 0 (USB disconnected)	0.996	mA
	GSM @ DRX = 2 (USB disconnected)	2.205	mA
	GSM @ DRX = 5 (USB disconnected)	1.635	mA
	GSM @ DRX = 5 (USB suspend)	TBD	mA
	GSM @ DRX = 9 (USB disconnected)	1.432	mA
	DCS @ DRX = 2 (USB disconnected)	2.11	mA
	DCS @ DRX = 5 (USB disconnected)	1.566	mA
	DCS @ DRX = 5 (USB suspend)	TBD	mA
	DCS @ DRX = 9 (USB disconnected)	1.401	mA
Sleep state	LTE-FDD @ PF = 32 (USB disconnected)	3.865	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.419	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.734	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.411	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.79	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.416	mA
	LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.75	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.417	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.95	mA

	EGSM900 @ DRX = 5 (USB connected)	28.133	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.254	mA
	LTE-FDD @ PF = 64 (USB connected)	28.097	mA
	LTE-TDD @ PF = 64 (USB disconnected)	13.331	mA
	LTE-TDD @ PF = 64 (USB connected)	28.127	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.2 dBm	231	mA
	EGSM900 3DL/2UL @ 31.3 dBm	344.7	mA
	EGSM900 2DL/3UL @ 29.2 dBm	395.6	mA
	EGSM900 1DL/4UL @ 28.3 dBm	406.9	mA
	DCS1800 4DL/1UL @ 30.1 dBm	156	mA
	DCS1800 3DL/2UL @ 28.5 dBm	213.7	mA
	DCS1800 2DL/3UL @ 26.4 dBm	244.9	mA
	DCS1800 1DL/4UL @ 25.1 dBm	252	mA
LTE data transfer	LTE-FDD B1 @ 23.2 dBm	630	mA
	LTE-FDD B3 @ 23.5 dBm	566	mA
	LTE-FDD B5 @ 23.4 dBm	570.9	mA
	LTE-FDD B8 @ 23.1 dBm	615.5	mA
	LTE-TDD B34 @ 23.01 dBm	307.1	mA
	LTE-TDD B38 @ 23.1 dBm	370.9	mA
	LTE-TDD B39 @ 22.95 dBm	279.6	mA
	LTE-TDD B40 @ 23.12 dBm	306.4	mA
	LTE-TDD B41 @ 23.37 dBm	415.3	mA
GSM voice call	EGSM900 PCL = 5 @ 33.27 dBm	250	mA
	EGSM900 PCL = 12 @ 19.42 dBm	92.2	mA
	EGSM900 PCL = 19 @ 6.21 dBm	62.8	mA

	DCS1800 PCL = 0 @ 30.24 dBm	175	mA
	DCS1800 PCL = 7 @ 16.2 dBm	75.4	mA
	DCS1800 PCL = 15 @ 0.87 dBm	57.7	mA

Table 35: EC200U-EU QuecOpen Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	29	μA
Sleep state	**AT+CFUN = 0** (USB disconnected)	1.159	mA
	GSM @ DRX = 2 (USB disconnected)	2.697	mA
	GSM @ DRX = 5 (USB disconnected)	2.138	mA
	GSM @ DRX = 5 (USB suspend)	3.694	mA
	GSM @ DRX = 9 (USB disconnected)	1.944	mA
	DCS @ DRX = 2 (USB disconnected)	2.697	mA
	DCS @ DRX = 5 (USB disconnected)	2.156	mA
	DCS @ DRX = 5 (USB suspend)	3.747	mA
	DCS @ DRX = 9 (USB disconnected)	1.988	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.715	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.955	mA
	LTE-FDD @ PF = 64 (USB suspend)	3.622	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.567	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.378	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.761	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.971	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.576	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.580	mA

	LTE-TDD @ PF = 256 (USB disconnected)	1.381	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	20.19	mA
	EGSM900 @ DRX = 5 (USB connected)	29.07	mA
	LTE-FDD @ PF = 64 (USB disconnected)	20.18	mA
	LTE-FDD @ PF = 64 (USB connected)	28.98	mA
	LTE-TDD @ PF = 64 (USB disconnected)	20.22	mA
	LTE-TDD @ PF = 64 (USB connected)	29.02	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.89 dBm	254	mA
	GSM850 3DL/2UL @ 30.9 dBm	383	mA
	GSM850 2DL/3UL @ 28.67 dBm	431	mA
	GSM850 1DL/4UL @ 26.54 dBm	448	mA
	EGSM900 4DL/1UL @ 32.55 dBm	231	mA
	EGSM900 3DL/2UL @ 31.3 dBm	344.7	mA
	EGSM900 2DL/3UL @ 29.2 dBm	395.6	mA
	EGSM900 1DL/4UL @ 28.3 dBm	406.9	mA
	DCS1800 4DL/1UL @ 30.1 dBm	156	mA
	DCS1800 3DL/2UL @ 28.5 dBm	213.7	mA
	DCS1800 2DL/3UL @ 26.4 dBm	244.9	mA
	DCS1800 1DL/4UL @ 25.1 dBm	252	mA
	PCS1900 4DL/1UL @ 29.93 dBm	153	mA
	PCS1900 3DL/2UL @ 27.99 dBm	219	mA
	PCS1900 2DL/3UL @ 25.94 dBm	249	mA
	PCS1900 1DL/4UL @ 23.87 dBm	261	mA
LTE data transfer	LTE-FDD B1 @ 23.4 dBm	607	mA
	LTE-FDD B3 @ 22.96 dBm	508	mA

	LTE-FDD B5 @ 23 dBm	492	mA
	LTE-FDD B7 @ 22.8 dBm	709	mA
	LTE-FDD B8 @ 23.1 dBm	558	mA
	LTE-FDD B20 @ 23 dBm	576	mA
	LTE-FDD B28 @ 23.3 dBm	586	mA
	LTE-TDD B38 @ 23.1 dBm	320.9	mA
	LTE-TDD B40 @ 23.12 dBm	286	mA
	LTE-TDD B41 @ 23.37 dBm	317	mA
GSM voice call	GSM850 PCL = 5 @ 33 dBm	246	mA
	GSM850 PCL = 12 @ 19.8 dBm	95	mA
	GSM850 PCL = 19 @ 6.7 dBm	64	mA
	EGSM900 PCL = 5 @ 33.27 dBm	250	mA
	EGSM900 PCL = 12 @ 19.42 dBm	92.2	mA
	EGSM900 PCL = 19 @ 6.21 dBm	62.8	mA
	DCS1800 PCL = 0 @ 30.24 dBm	175	mA
	DCS1800 PCL = 7 @ 16.2 dBm	75.4	mA
	DCS1800 PCL = 15 @ 0.87 dBm	57.7	mA
	PCS1900 PCL = 0 @ 29.8 dBm	168	mA
	PCS1900 PCL = 7 @ 16.6 dBm	78	mA
	PCS1900 PCL = 15 @ 0.8 dBm	59	mA

5.5. RF Output Power

The following table shows the RF output power of EC200U series QuecOpen module.

Table 36: EC200U-CN RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm±2 dB	5 dBm±5 dB
DCS1800	30 dBm±2 dB	0 dBm±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm±2 dB	< -39 dBm

Table 37: EC200U-EU RF Output Power

Frequency	Max.	Min.
GSM850	33 dBm±2 dB	5 dBm±5 dB
EGSM900	33 dBm±2 dB	5 dBm±5 dB
DCS1800	30 dBm±2 dB	0 dBm±5 dB
PCS1900	30 dBm±2 dB	0 dBm±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 6 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3 GPP TS 51.010-1*.

5.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of EC200U series QuecOpen module.

Table 38: EC200U-CN QuecOpen Conducted RF Receiving Sensitivity

Frequency	Primary	3 GPP
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109.5 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99.6 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-TDD B34 (10 MHz)	-99.2 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-98.8 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-99.5 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-99.4 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.9 dBm	-94.3 dBm

Table 39: EC200U-EU QuecOpen Conducted RF Receiving Sensitivity

Frequency	Primary	3 GPP
GSM850	-109.5 dBm	-102.0 dBm
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109 dBm	-102.0 dBm
PCS1900	-109 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-97.8 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-94.3 dBm

LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-96.8 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.8 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-98.3 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98 dBm	-94.3 dBm

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 40: Electrostatics Discharge Characteristics (25ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05 mm.

6.1. Mechanical Dimensions of the Module

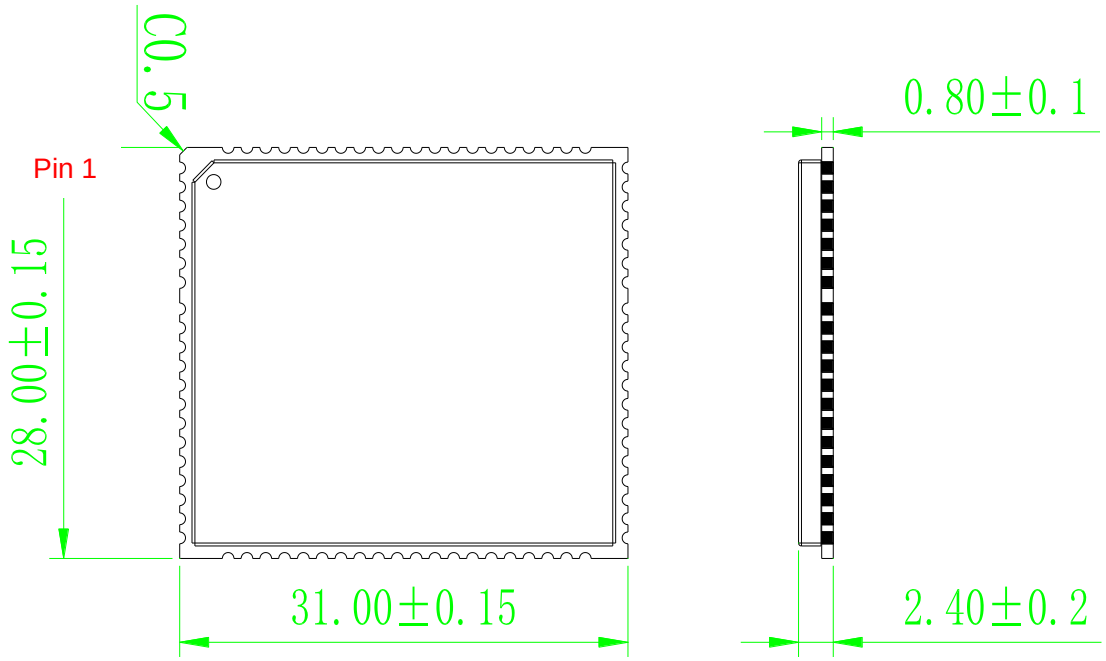


Figure 35: Module Top and Side Dimensions

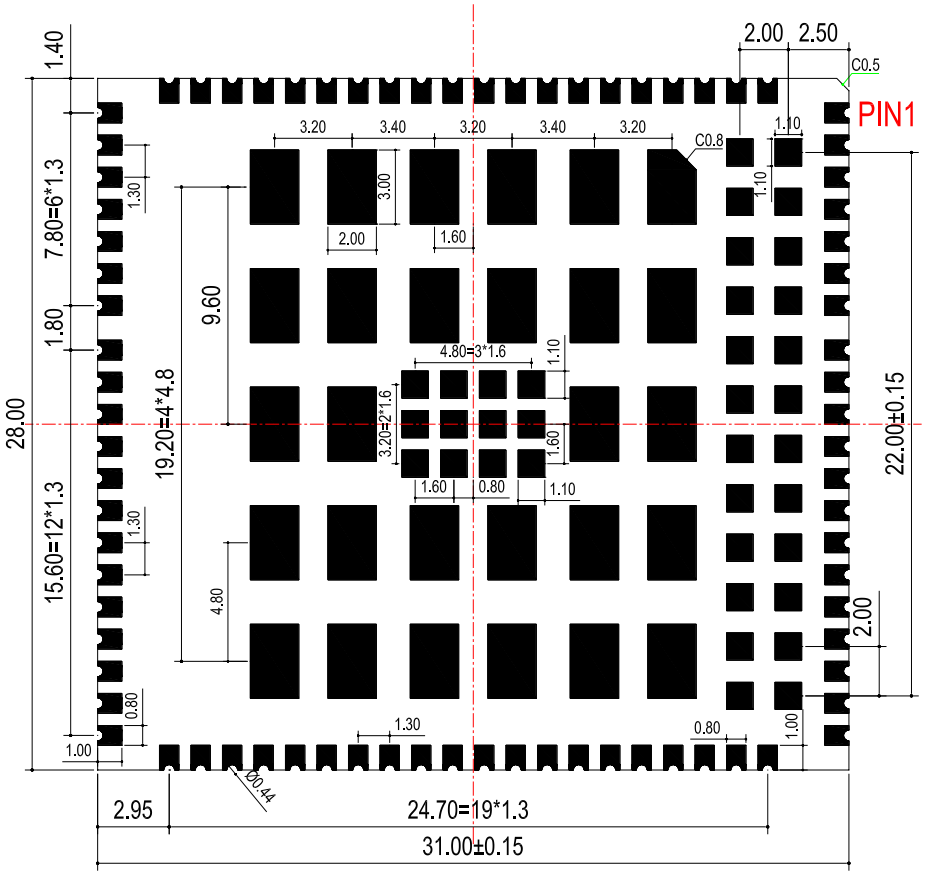


Figure 36: Module Bottom Dimensions

NOTES

The flatness of Quectel's EC200U series QuecOpen module meets the requirements of the "JEITA ED-7306" standard.

6.2. Recommended Footprint

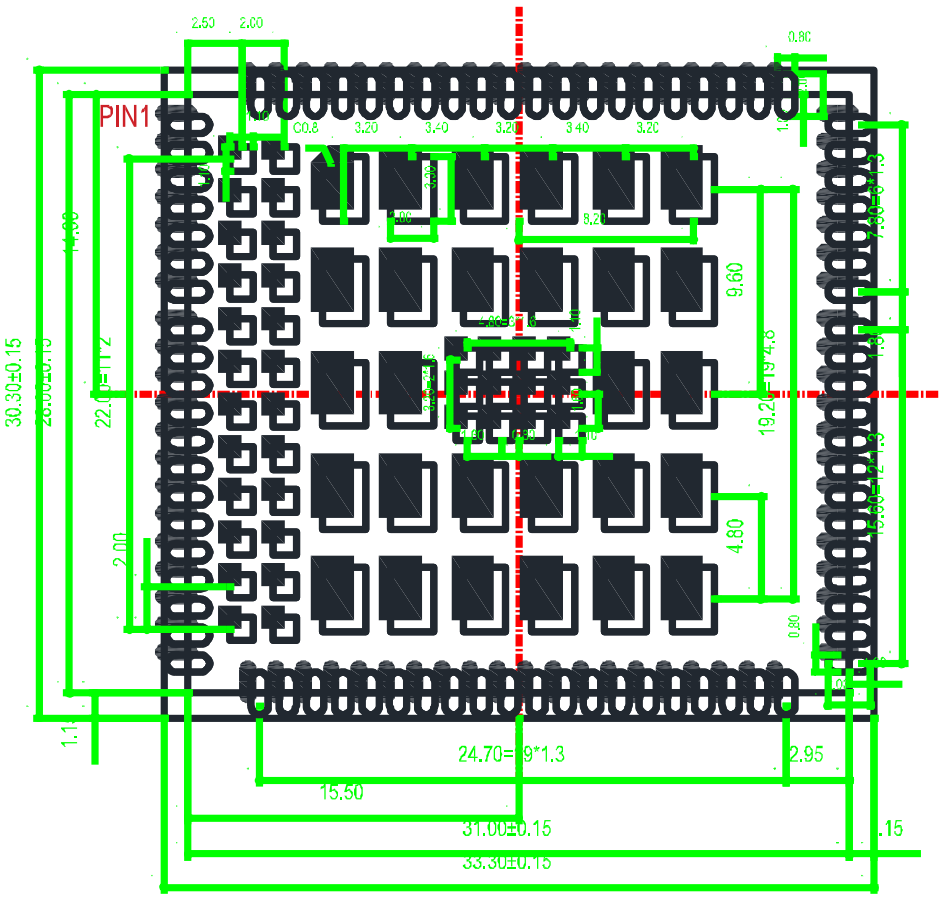


Figure 37: Recommended Footprint (Top View)

NOTES

For easy maintenance of the module, please keep about 3 mm between the module and other components in the host PCB.

6.3. Design Effect Drawings of the Module

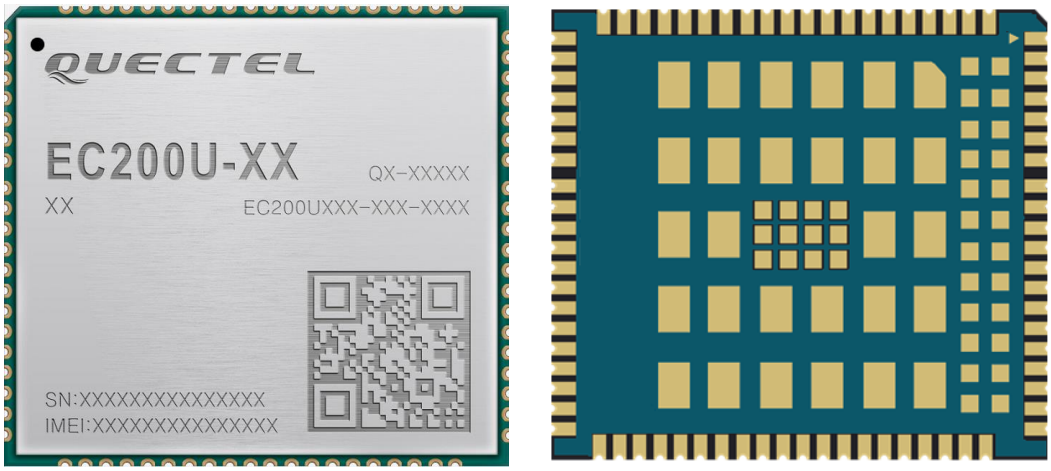


Figure 38: Top & Bottom View of the module

NOTE

These are renderings of EC200U series QuecOpen module. For authentic appearance, please refer to the module that you receive from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

EC200U series QuecOpen is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage
requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours 1) in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:
   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be ut in a dry environment such as in a drying oven.

NOTE

1. This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to IPC/JEDEC J-STD-033 or the relative moisture is over 60%, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the package of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, see IPC/JEDEC J-STD-033 for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm~0.20 mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238ºC~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

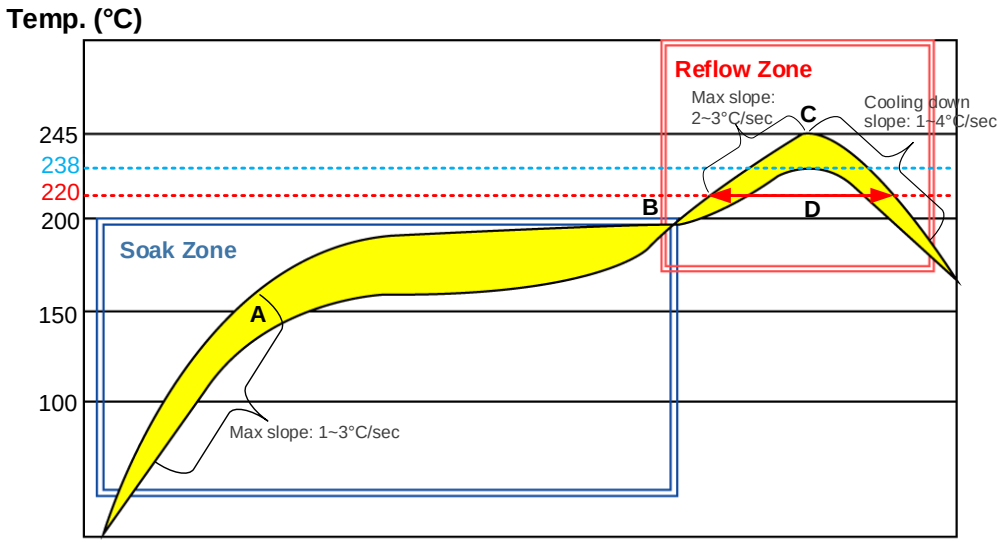


Figure 39: Reflow Soldering Thermal Profile

Table 41: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/sec
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 sec
Reflow Zone	
Max slope	2 to 3 °C/sec
Reflow time (D: over 220 °C)	45 to 70 sec
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

7.3. Packaging

EC200U series QuecOpen is packaged in tap and reel carriers. Each reel is 11.88 m long and contains 250 pcs modules. The figure below shows the package details, measured in mm.

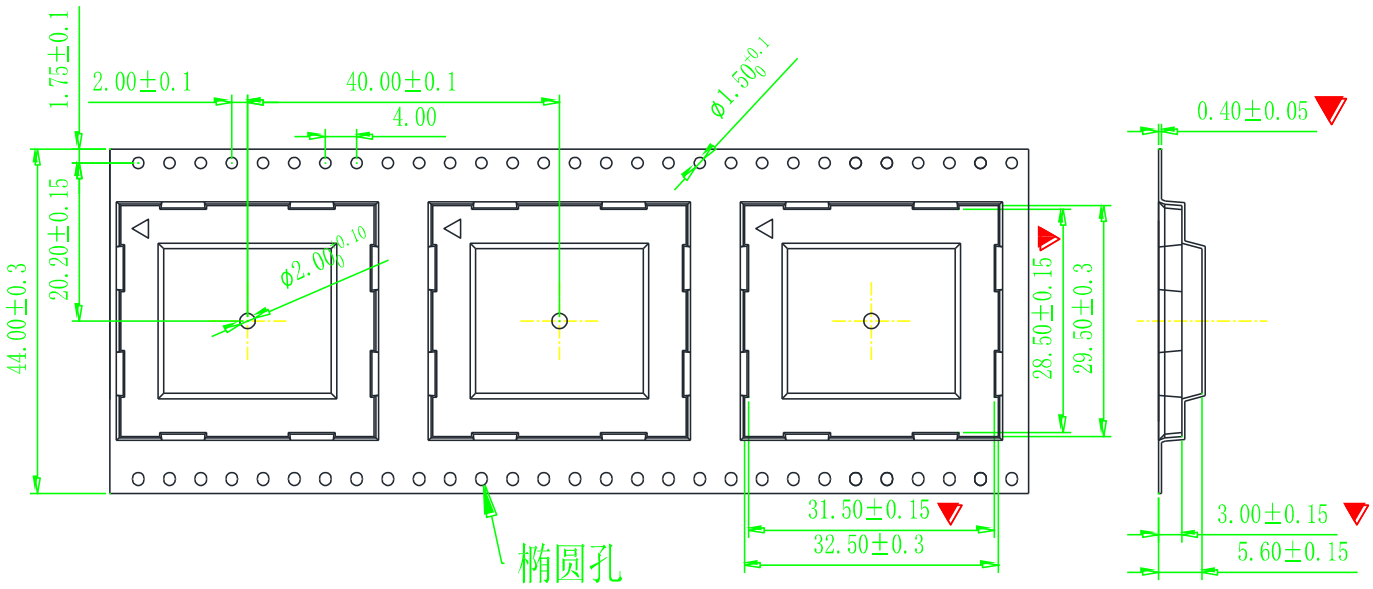


Figure 40: Tape and Reel Specifications

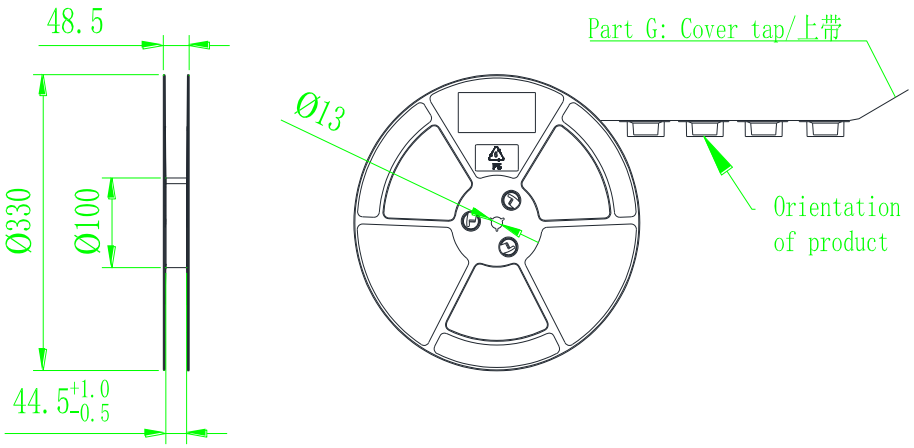


Figure 52: Reel Specifications

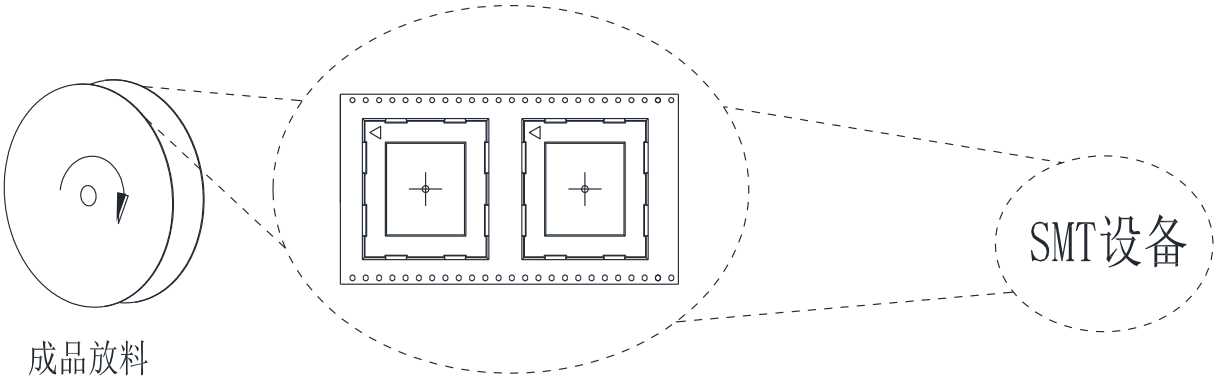


Figure 41: Tape and Reel Directions

8 Appendix A References

Table 42: Related Documents

SN	Document Name	Remark
[1]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules
[2]	Quectel_LTE_Standard_AT_Commands_Manual	AT commands manual for AT commands manual
[3]	Quectel_RF_Layout_Application_Note	RF layout application note
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

Table 43: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DMA	Direct Memory Access
DL	Downlink
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High-Speed Down Link Packet Access
HSPA	High-Speed Packet Access
HSUPA	High-Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board

PDU	Protocol Data Unit
PF	Paging Frame
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RGB	Red, Green, Blue
SIMO	Single Input Multiple Output
SM	Smart Media
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Normal Voltage Value
Vmin	Minimum Voltage Value

$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{OH}max$	Maximum Output High Level Voltage Value
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
$V_{OL}min$	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 44: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Thirty-three classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 45: GPRS Multi-slot Classes

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6