EC200G-CN

Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-06-19	Denny QIN/ Kleene QIN	Creation of the document
1.0	2023-09-21	Denny QIN/ Kleene QIN	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC200G-CN module, including block diagrams of module design, power supply, USIM, UART, analog audio, and antenna.

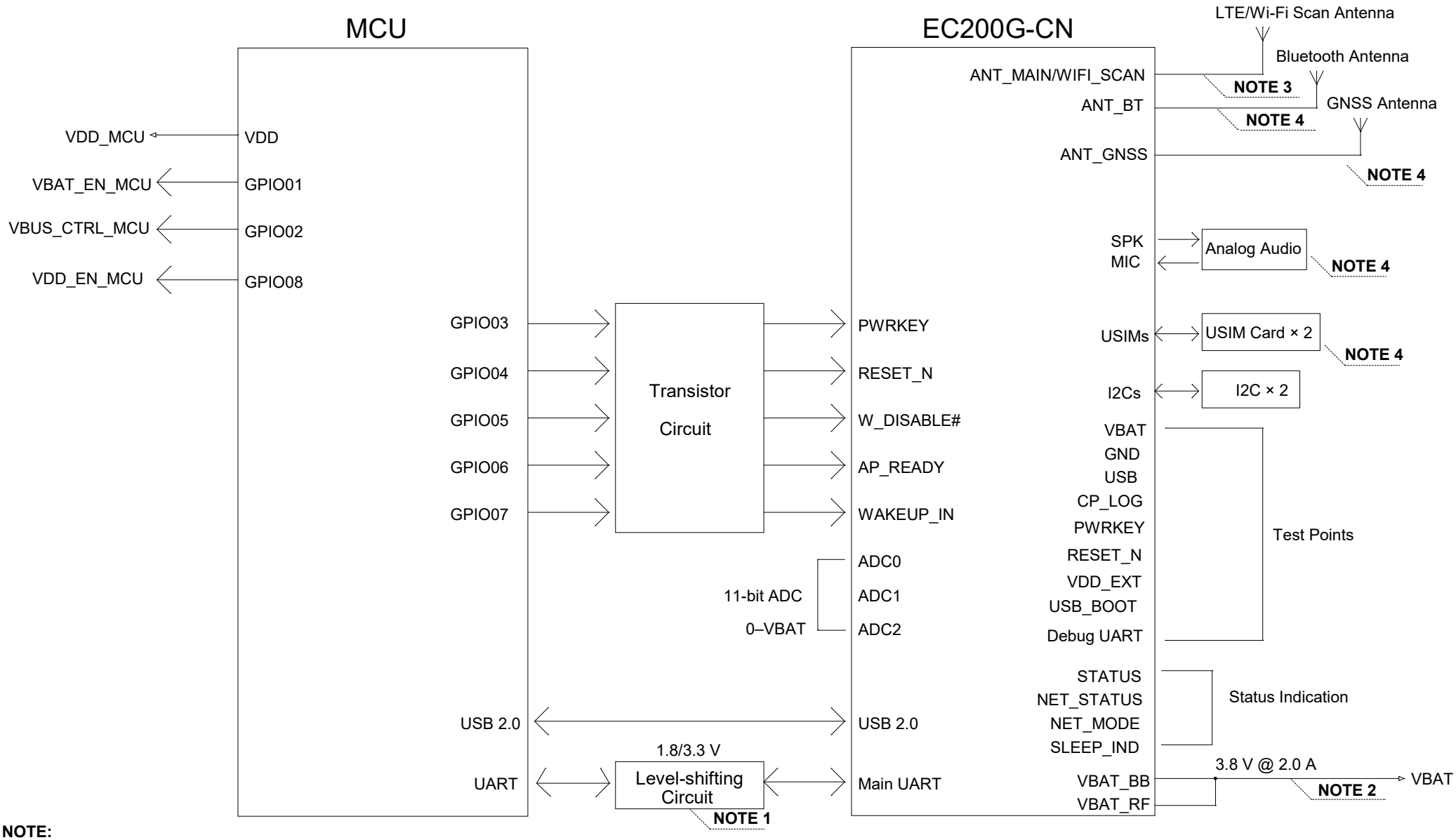
1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
3. The module supports Wi-Fi scan function, which shares the same antenna interface with main antenna. The two functions cannot be used at the same time.
4. USIM2, analog audio, Bluetooth and GNSS functions are optional for the module.

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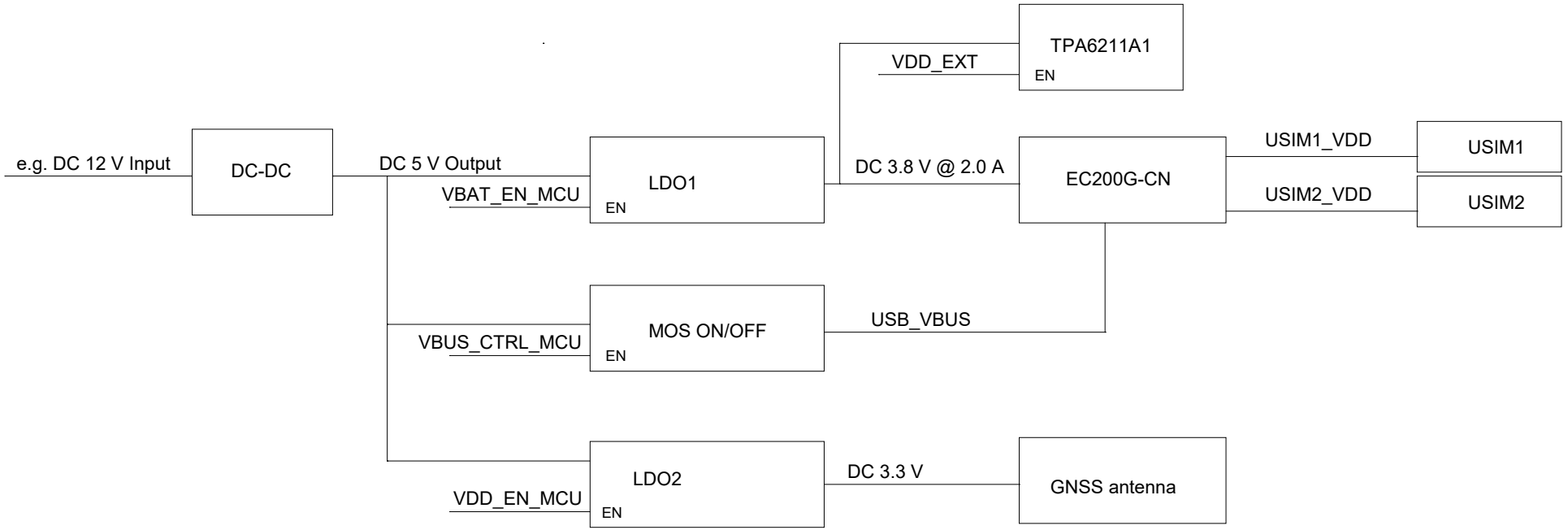
Power System Block Diagram



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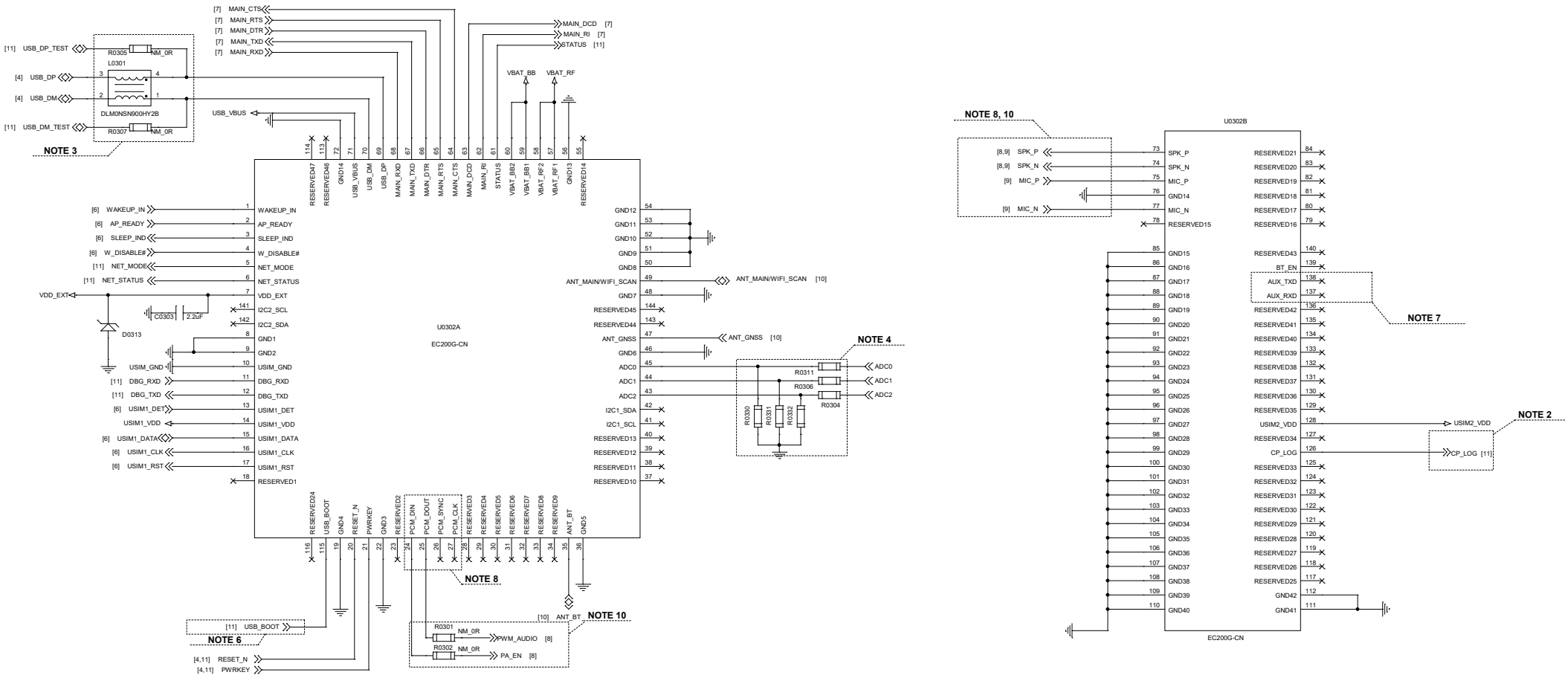
Module Interfaces



NOTE:

1. Connect all GND pins to ground, and keep unused and RESERVED pins unconnected. The ground plane should be placed as close to the module layer as possible. At least four-layer board design is recommended.
2. A test point must be reserved for CP_LOG pin to capture CP logs.
3. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI spurious transmission. Additionally, test points must be reserved over USB_DP/_DM for firmware upgrades, and it is recommended to minimize extra trace stubs. Place L0301 and the two resistors, R0305 and R0307, close to the module to ensure USB signal integrity.
4. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistor in series.
5. It is strongly recommended to reserve a Π-type matching circuit for the antenna circuit, which is convenient for future debugging. The single-ended impedance of the RF antenna is 50 Ω.
6. If the emergency download function is not used, do not pull up or pull down the USB_BOOT pin, and keep it open before the module is successfully turned on.
7. The connection method of the auxiliary UART is the same as that of the main UART. For details, see Sheet "UART Interface Design".
8. PCM and analog audio interfaces cannot be used at the same time. Contact Quectel Technical Support for details.
9. Test points must be reserved for DBG_TXD/_RXD and USB_VBUS. It is recommended to reserve test points for USB_BOOT, VDD_EXT, VBAT and PWRKEY. If RESET_N is unused, it is recommended to reserve a test point.
10. Choose one of the PCM, PWM audio and analog audio interfaces for implementing audio function.

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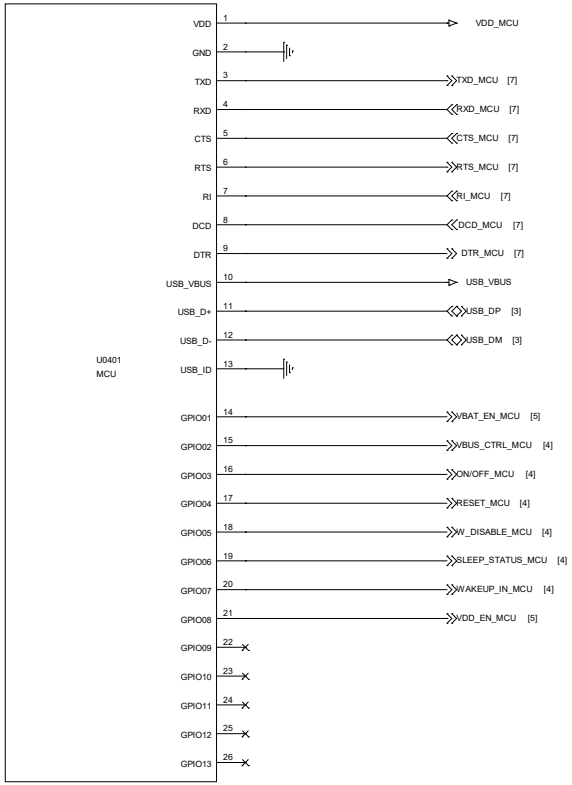
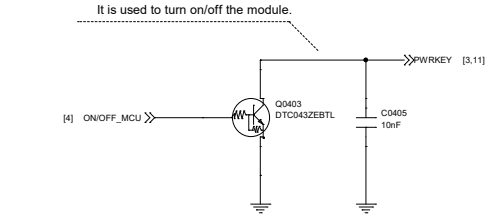
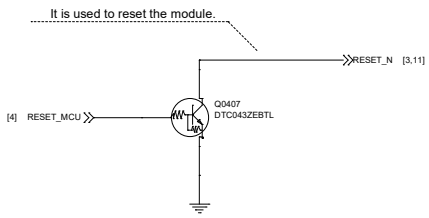
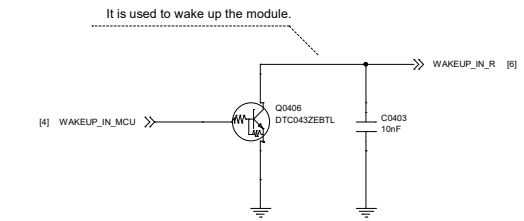
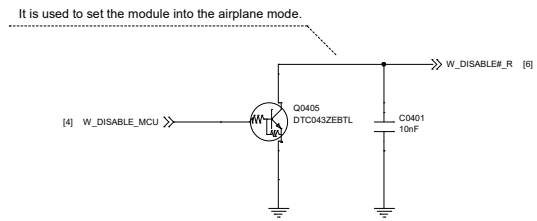
MCU Interfaces

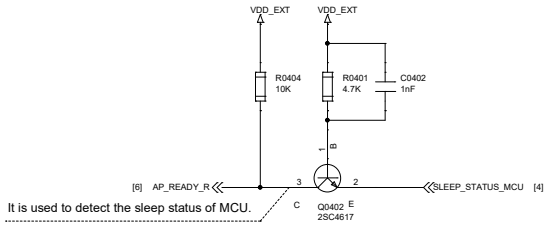


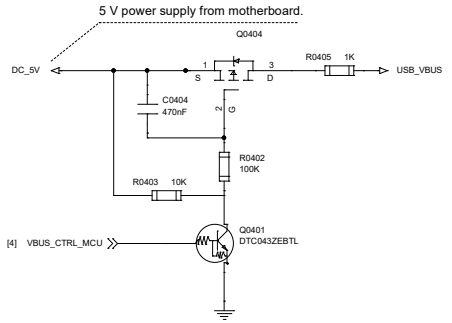












NOTE:

1. If the power domain of your MCU (U0401) is aslo 1.8 V, the level-shifting circuit is not necessary as it matches the 1.8 V power domain of the module's GPIO interfaces.
2. The module's USB 2.0 interface can only serve as a slave device and supports high-speed and full-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL_MCU to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.

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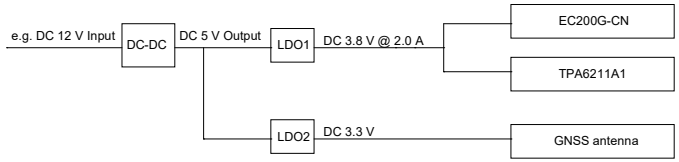
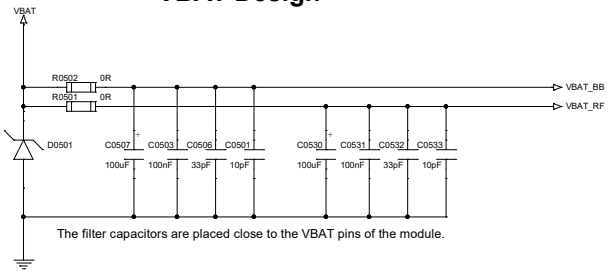
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDO to convert it to 3.8 V.



VBAT Design



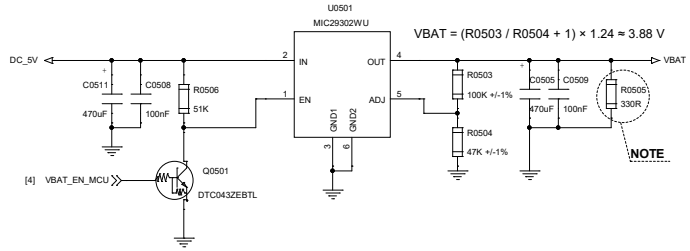
The filter capacitors are placed close to the VBAT pins of the module.

NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
2. The width of VBAT_BB trace should be at least 2 mm and the width of VBAT_RF trace should be at least 2.5 mm.
3. VBAT_BB and VBAT_RF pins should be divided into two separated paths in star configuration.
4. The recommended operating voltage range for VBAT is 3.3 V–4.3 V, with a typical vaule of 3.8 V.

LDO Application

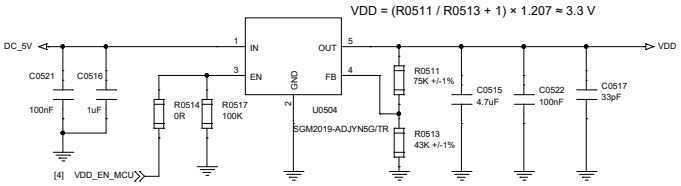
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current should exceed 10 mA.

Power Supply for GNSS Antenna



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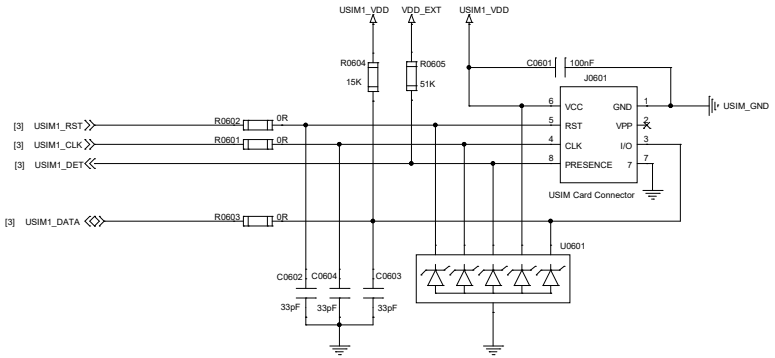
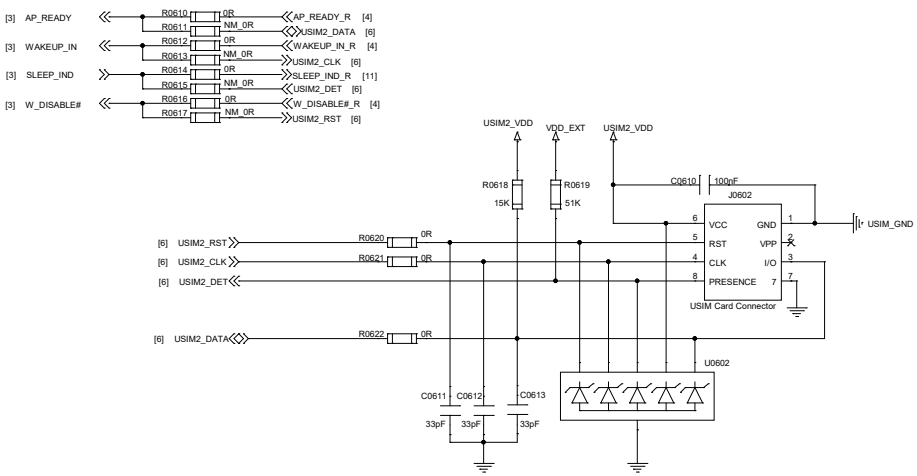
USIM Interface Design

USIM1



USIM2



NOTE:

1. It is recommended to use U0601 and U0602 for effective ESD protection with a parasitic capacitance below 15 pF.
2. The GND of the USIM card connector is recommended to be connected to the module's USIM_GND to avoid being interfered by the ground of USIM card connector, and can also be connected to the ground of PCB if your PCB has a complete ground plane.
3. For USIM_DATA, it is recommended to add 15 kΩ pull-up resistors R0604 and R0618 near the USIM card connector to improve the anti-jamming capability of the USIM card.
4. R0601–R0603 and R0620–R0622 are used for debugging; capacitors C0602–C0604 and C0611–C0613 are used for filtering out RF interference.
5. C0601 and C0610's capacitance should be less than 1 μF and they should be placed close to the USIM card connector.
6. For layout and routing, see the hardware design document of the module.
7. The USIM2 function of the module is optional. Contact Quectel Technical Support for details.

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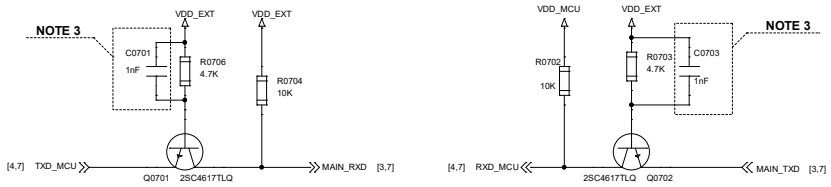
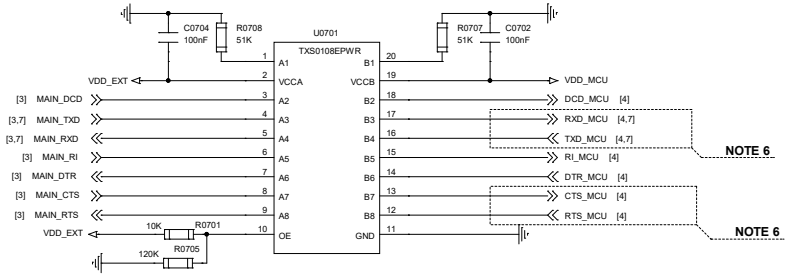
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution

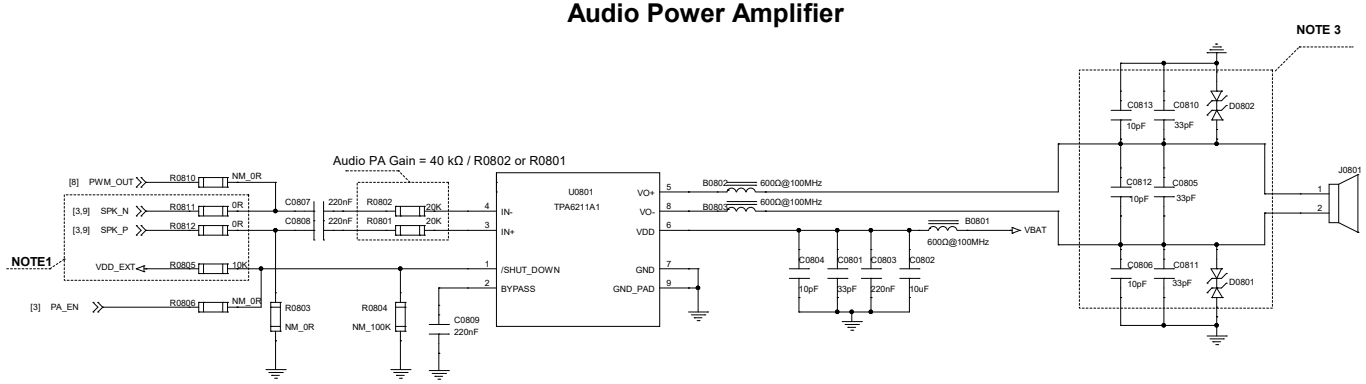


NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps. The capacitors C0701 and C0703 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD interface. MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD interface.
5. The auxiliary UART design is the same as the main UART.
6. The RTS of the module is connected to the RTS of the MCU, and the CTS of the module is connected to the CTS of the MCU, and pay attention to the signal direction.
   The TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

Analog Audio Design - Part 1

Audio Power Amplifier

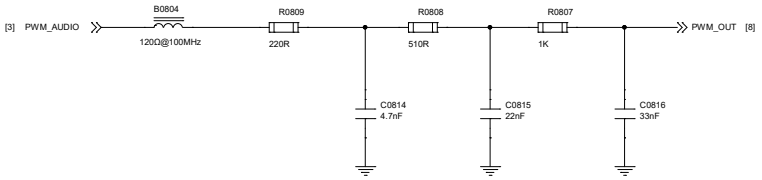


NOTE:

1. SPK_N and SPK_P are differential output channels. When the channels are turned on or off, it is possible for module to emit a pop sound, which can be eliminated by controlling the enable pin of the audio PA. For details, contact Quectel Technical Support.
2. Choose the audio power amplifier with appropriate power according to the actual needs.
3. Place filter capacitors and ESD protection components close to the loudspeaker and the selection of ESD protection components is related to the selection of audio power amplifiers.
   Ensure that the output voltage of the audio power amplifier is within the maximum reverse working voltage range of the ESD protection components.

	SPK	PWM
R0810	NM	0 Ω
R0811	0 Ω	NM
R0812	0 Ω	NM
R0805	10 kΩ	NM
R0806	NM	0 Ω
R0803	NM	0 Ω

PWM (RC-filter Circuit)

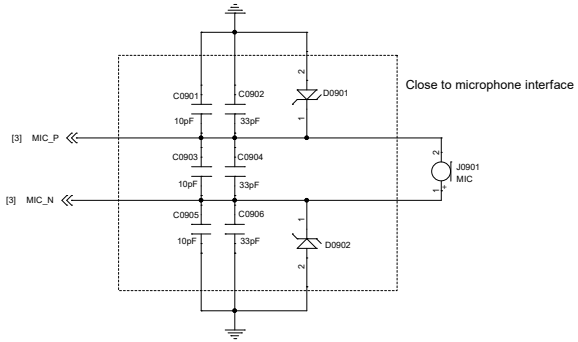


NOTE:

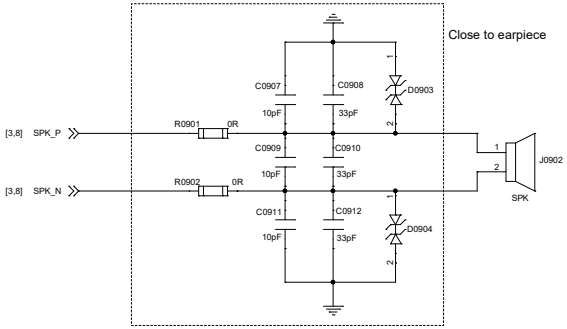
1. You can reserve a second-order or third-order RC low-pass filter circuit, and the capacitance and resistance need to be adjusted according to the audio effect and the matched audio PA. This circuit is for reference only.
2. You can use low-pass filters such as first-order, second-order or third-order RC or LC according to the needs.

Analog Audio Design - Part 2

Microphone Application



Earpiece Application



NOTE:

1. Route the MIC and SPK signal traces as differential pairs.
2. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference.
3. If the limited output power of SPK channels does not meet your needs, install an external power amplifier.

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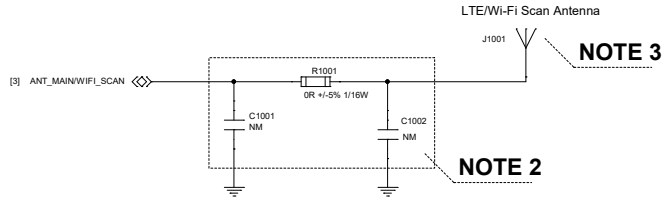
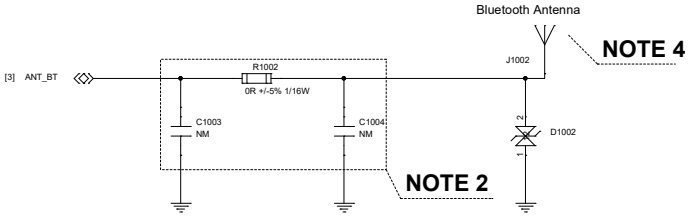
RF Interface Design

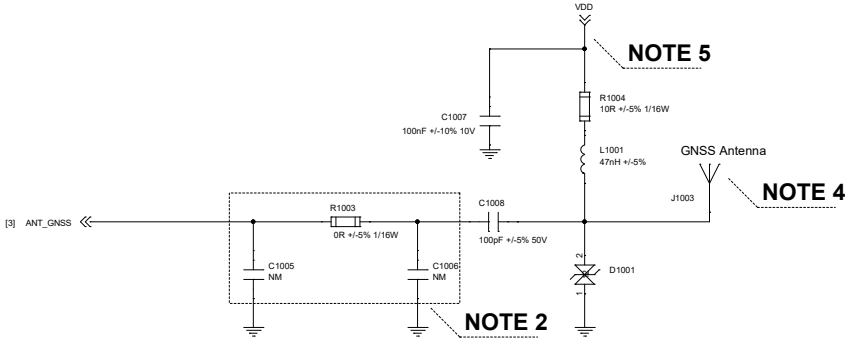
LTE/Wi-Fi Scan Antenna Interface



Bluetooth Antenna Interface



GNSS Antenna Interface



NOTE:

1. The single-ended impedance of the RF antenna is 50 Ω.
2. It is recommended to reserve a π-type matching circuit at antenna interfaces.
3. The Wi-Fi scan function shares the same antenna interface with main antenna. The two functions cannot be used at the same time.
4. Bluetooth and GNSS functions are optional for the module.
5. For active antennas, select an external LDO according to the active antenna types. In case of passive antennas, the VDD circuit is not necessary.
6. The junction capacitance of the ESD protection components on the antenna interfaces is recommended to be less than 0.05 pF.
7. The external active GNSS antenna power supply voltage range is 2.8 V–4.3 V, with a typical value of 3.3 V.

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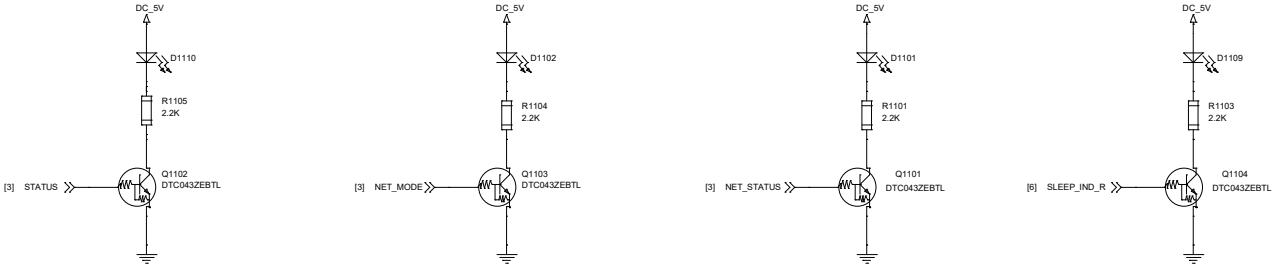
Other Designs

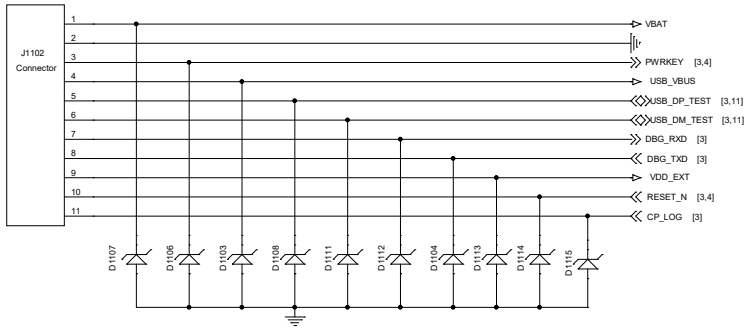
Indicators



NOTE:

1. For more details about STATUS, NET_MODE, NET_STATUS and SLEEP_IND_R, see the hardware design document of the module.
2. To minimize the module's power consumption during the sleep mode of your device, replace the power supply DC_5V of the STATUS, NET_MODE, NET_STATUS and SLEEP_IND_R indicators with externally controllable sources and turn off the indicators when the module is in sleep mode.

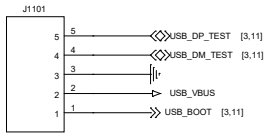
Reserved Test Points



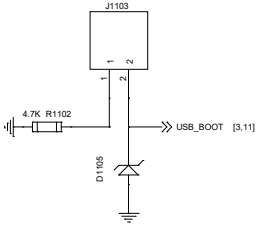
NOTE:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection components on the USB data traces should not exceed 2 pF.
4. The baud rate of debug UART interface is fixed at 2 Mbps. The debug UART interface supports a 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.

USB Interface Design



USB_BOOT Interface Design



NOTE:

1. Before turning on the module, pull USB_BOOT down to GND to activate the emergency download mode. This mode enables firmware upgrades via the USB interface.
2. Be sure to design the circuit to control the pull-down and floating state of USB_BOOT.

Quectel Wireless Solutions		
PROJECT: EC200G-CN		VER: 1.0
DRAWN BY: Denny QIN/Kleene QIN	CHECKED BY: Vane WANG	SIZE: A2
DATE: Thursday, September 21, 2023	SHEET: 11OF 11	