

am^U TCS3448

Datasheet

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TCS3448 14-channel multi-spectral sensor

1 General description

The TCS3448 is a 14-channel highly versatile, multi-purpose spectral light sensor. It is optimized to sense spectral components of ambient light in the visible range. Such spectral information is used for camera enhancement (CCT, AWB, exposure time).

The spectral response is defined by individual channels covering approximately 380 nm to 1000 nm with 11 channels centered in the visible spectrum (VIS), plus one near-infrared (NIR) and a clear channel. Applications can be assisted to allow classification of ambient light and an integrated flicker detection channel that can automatically flag ambient light flicker at 50/60 Hz as well as buffer data for externally calculating other flicker frequencies.

TCS3448 integrates high-precision optical interference filters directly deposited on photodiodes which are embedded in CMOS silicon. A built-in aperture controls the light entering the sensor array to increase accuracy. A programmable digital GPIO and LED driver enable light source and trigger/sync control. Device control and spectral data access is implemented through a serial I²C 1.2 V/1.8 V interface. The device is available in an ultra-low profile package with dimensions of 3.1 mm x 2 mm x 1 mm.

1.1 Key benefits & features

The benefits and features of TCS3448, 14-channel multi-spectral sensor are listed below:

Table 1: Added value of using TCS3448

| Benefits | Features |
|--|---|
| Highly versatile multi-purpose spectral sensor | <ul style="list-style-type: none">• 14 channels between 380 nm and 1000 nm• Reflective, transmissive and emissive applications |
| Highest sensitivity | <ul style="list-style-type: none">• Enables ultra-low light operation• Enables operation behind dark glass |
| Low power consumption and minimum I ² C traffic | <ul style="list-style-type: none">• 1.8 V supply voltage• 1.2 V/1.8 V I²C bus voltage• Configurable sleep mode• Interrupt-driven device |
| Ultra-high integration | <ul style="list-style-type: none">• On chip interference filter technology• Integrated LED driver and 6 ADCs• 3.1 mm x 2 mm x 1 mm package outline |

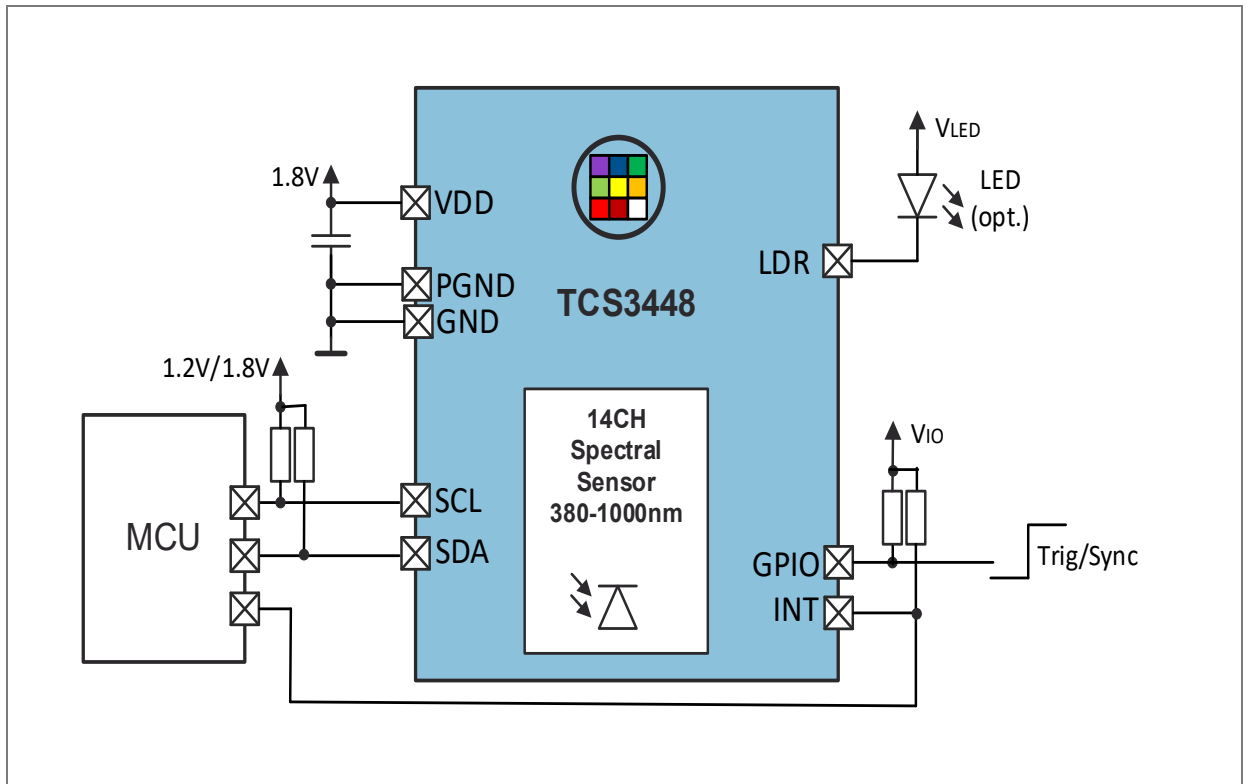
1.2 Applications

- Accurate ambient light measurement for camera enhancement.
- Calculation of reconstructed spectra, light source ID and ambient light flicker.
- Highly accurate CCT and LUX measurement.

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of TCS3448



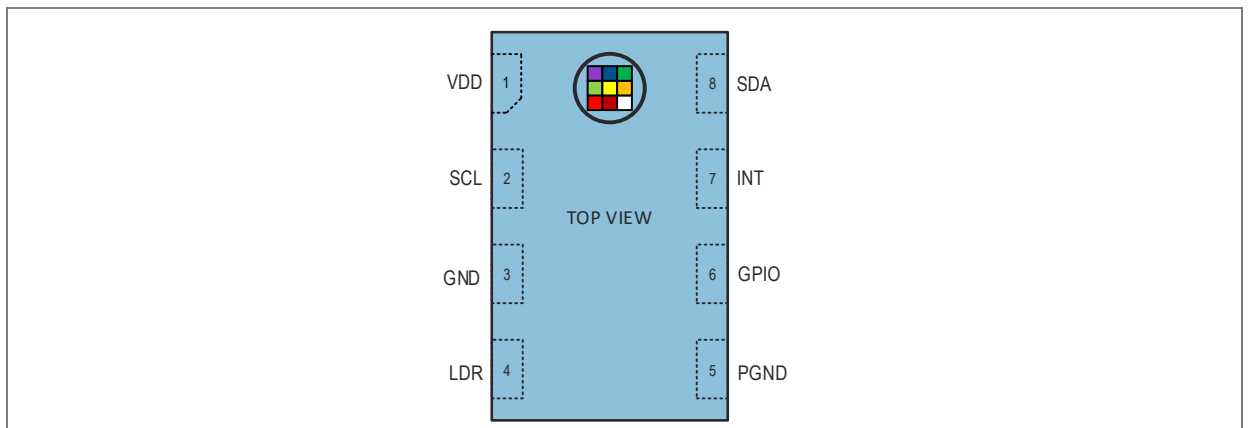
2 Ordering information

| Product type | Ordering code | Address | Delivery form | Delivery quantity |
|---------------|---------------|---------|---------------------|-------------------|
| TCS34488-DOLT | Q65113A9196 | 0x59 | Tape & reel 13-inch | 10000 pcs/reel |
| TCS34488-DOLM | Q65115A3011 | 0x59 | Tape & reel 7-inch | 500 pcs/reel |

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of TCS3448 (Top View)



3.2 Pin description

Table 2: Pin description of TCS3448

| Pin number | Pin name | Pin type ⁽¹⁾ | Description |
|------------|----------|-------------------------|--|
| 1 | VDD | P | Positive supply voltage terminal. |
| 2 | SCL | DI | Serial interface clock signal line for I ² C interface. Connect pull up resistor to 1.2 V or 1.8 V. |
| 3 | GND | P | Ground. All voltages referenced to GND. |
| 4 | LDR | A_I/O | LED current sink input. If not used leave pin open. |
| 5 | PGND | P | Ground. All voltages referenced to GND. |
| 6 | GPIO | D_I/O | General purpose input/output. Pin is used to select 1.2 V or 1.8 V I ² C I/O voltage. Please refer to chapter "Selection of I ² C bus interface voltage". |
| 7 | INT | DO_OD | Interrupt. Open drain output active low. Connect pull up resistor to 1.8 V. If not used leave pin unconnected. |
| 8 | SDA | D_I/O | Serial interface data signal line for I ² C interface. Connect pull up resistor to 1.2 V or 1.8 V. |

(1) Explanation of abbreviations:

DI = Digital Input, D_I/O = Digital Input/Output, DO_OD = Digital output, Open drain, P = Power pin, A_I/O = Analog pin

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages with respect to GND/PGND. Device parameters are guaranteed at $V_{DD}=1.8\text{ V}$ and $T_A=25\text{ °C}$ unless otherwise noted.

Table 3: Absolute maximum ratings of TCS3448

| Symbol | Parameter | Min | Max | Unit | Comments |
|--|------------------------------------|------|-------|------|------------------------------------|
| Electrical parameters | | | | | |
| V_{DD} / V_{GND} | Supply voltage to ground | -0.3 | 1.98 | V | Applicable for pin VDD |
| V_{ANA_MAX} | Analog pins | -0.3 | 3.6 | V | Applicable for pin LDR |
| V_{IO} | Digital pins | -0.3 | 3.6 | V | Applicable for pins GPIO and INT |
| V_{BUS} | Digital pins | -0.3 | 1.98 | V | Applicable for pins SCL and SDA |
| I_{SCR} | Input current (latch-up immunity) | | ±100 | mA | AEC-Q100-004E |
| I_O | Output terminal current | -1 | 20 | mA | |
| Electrostatic discharge | | | | | |
| ESD_{HBM} | Electrostatic discharge HBM | | ±2000 | V | JS-001-2017 |
| ESD_{CDM} | Electrostatic discharge CDM | | ±500 | V | JS-002-2018 |
| Temperature ranges and storage conditions | | | | | |
| T_A | Operating ambient temperature | -30 | 85 | °C | |
| T_{STRG} | Storage temperature range | -40 | 85 | °C | |
| T_{BODY} | Package body temperature | | 260 | °C | IPC/JEDEC J-STD-020 ⁽¹⁾ |
| R_{HNC} | Relative humidity (non-condensing) | 5 | 85 | % | |
| MSL | Moisture sensitivity level | | 3 | | Maximum floor life time of 168h |

- (1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at $V_{DD}=1.8\text{ V}$ and $T_A=25\text{ °C}$ unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Table 4: Electrical characteristics of TCS3448

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|---|---|-----------------------|-----|----------------------|------|
| V_{DD} | Supply voltage | | 1.7 | 1.8 | 1.98 | V |
| T_A | Operating free-air temperature ⁽¹⁾ | | -30 | 25 | 85 | °C |
| Power consumption | | | | | | |
| IDD | Supply current ⁽²⁾ | $V_{DD}=1.8\text{ V}; T_A=25\text{ °C}$ Active mode ⁽³⁾ | | 210 | 280 | μA |
| | | $V_{DD}=1.8\text{ V}; T_A=25\text{ °C}$ Idle mode ⁽⁴⁾ | | 40 | 60 | μA |
| | | $V_{DD}=1.8\text{ V}; T_A=25\text{ °C}$ Sleep mode ⁽⁵⁾ | | 0.7 | 5 | μA |
| Digital pins | | | | | | |
| Vbus1.2 | Vbus I/O voltage | $V_{bus} = 1.2\text{ V}$ | 1.08 | 1.2 | 1.32 | V |
| Vbus1.8 | Vbus I/O voltage | $V_{bus} = 1.8\text{ V}$ | 1.62 | 1.8 | 1.98 | V |
| VIL-INT/GPIO | INT and GPIO input low voltage | | | | 0.54 | V |
| VIH-INT/GPIO | INT and GPIO input high voltage | | 0.84 | | | V |
| VIL1-SCL/SDA | SCL, SDA input low voltage | $V_{bus} = 1.2\text{ V or }1.8\text{ V}$ | $-0.1 \times V_{bus}$ | | $0.3 \times V_{bus}$ | V |
| VIH-SCL/SDA | SCL, SDA input high voltage | $V_{bus} = 1.2\text{ V or }1.8\text{ V}$ | $0.7 \times V_{bus}$ | | | V |
| VOL | INT, SDA output low voltage | 6 mA sink current | | | 0.4 | V |
| CI | Input pin capacitance | | | | 10 | pF |
| Ileak | Leakage current into SCL, SDA, INT pins | | -5 | | 5 | μA |
| GPIO | | | | | | |
| CLOAD | Maximum capacitive load GPIO | | | | 20 | pF |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------|------------------------------------|-----|-----|-----|------|
| LED driver | | | | | | |
| V_LDR | LDR compliance voltage | I_LDR= 4 mA ; LED_HALF = "0" | | | 240 | mV |
| | | I_LDR= 4 mA ; LED_HALF = "1" | | | 130 | |
| | | I_LDR = 134 mA ; LED_HALF = "0" | | | 280 | |
| | | I_LDR = 134 mA ; LED_HALF = "1" | | | 180 | mV |

- (1) While the device is operational across the temperature range, functionality will vary with temperature.
- (2) Supply current values are shown at the VDD pin and do not include current through pin LDR.
- (3) Active state occurs during active integration (PON = "1" ; ALS_EN = "1"). If wait is enabled (WEN = "1"), supply current is lower during the wait period.
- (4) Idle state occurs when PON = "1" and all functions are disabled.
- (5) Sleep state occurs when PON = "0" and I²C bus is idle. If I²C traffic is active device automatically enters idle mode.

6 Optical characteristics

Parameters listed under Test Level 4 are guaranteed with production tests and SQC (Statistical Quality Control). Parameters listed under Test Level 3 are measured in-line with transparent monitor glasses. Parameters listed under Test Level 2 are measured in lab bench characterization. Parameters listed under Test Level 1 are guaranteed by design. All Test Levels are measured with $V_{DD} = 1.8\text{ V}$ and $T_A = 25\text{ °C}$ unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Table 5: TCS3448 filter wavelength summary

| Channel | Peak wavelength [nm] ⁽¹⁾⁽²⁾ | | | Full width half maximum [nm] | Test level |
|---------|--|-------------------|-------|------------------------------|------------|
| | (min) | λ_p (typ) | (max) | (typ) | |
| F1 | 397 | 407 | 417 | 28 | 2+3 |
| F2 | 414 | 424 | 434 | 29 | 2+3 |
| FZ | 440 | 450 | 460 | 67 | 2+3 |
| F3 | 463 | 473 | 483 | 38 | 2+3 |
| F4 | 506 | 516 | 526 | 48 | 2+3 |
| FY | 550 | 560 | 570 | 123 | 2+3 |
| F5 | 536 | 546 | 556 | 44 | 2+3 |
| FXL | 586 | 596 | 606 | 93 | 2+3 |
| F6 | 626 | 636 | 646 | 58 | 2+3 |
| F7 | 677 | 687 | 697 | 63 | 2+3 |
| F8 | 738 | 748 | 758 | 77 | 2+3 |
| NIR | 845 | 855 | 865 | 61 | 2+3 |

- (1) Peak Wavelength and Full Width Half Max is validated by smoothed/averaged results from spectral scans under diffused light with a reference monochromator in ams OSRAM optical lab. Please observe that comparison measurements between two monochromators in different optical labs will first require correlation measurements between these two monochromators.
- (2) Repeated temperature stress during e.g. soldering may alter measurements results and optical performance.

Table 6: TCS3448 irradiance responsivity of spectral channels, AGAIN: 1024x, int. time: 27.8 ms

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Conditions | Min | Typ | Max | Unit | Test level |
|--------------------|---|--|------|------|-------|--------|------------|
| R _{e_F1} | Irradiance responsivity channel F1 | LED_396 nm ; Ee= 155 mW/m ² LED_408 nm ; Ee= 155 mW/m ² | 6698 | 8930 | 11162 | counts | 4 |
| R _{e_F2} | Irradiance responsivity channel F2 | LED_408 nm ; Ee= 155 mW/m ² LED_448 nm ; Ee= 155 mW/m ² | 1892 | 2522 | 3152 | counts | 4 |
| R _{e_FZ} | Irradiance responsivity channel FZ | LED_428 nm ; Ee= 155 mW/m ² LED_480 nm ; Ee= 155 mW/m ² | 2124 | 2832 | 3540 | counts | 4 |
| R _{e_F3} | Irradiance responsivity channel F3 | LED_448 nm ; Ee= 155 mW/m ² LED_500 nm ; Ee= 155 mW/m ² | 711 | 947 | 1183 | counts | 4 |
| R _{e_F4} | Irradiance responsivity channel F4 | LED_500 nm ; Ee= 155 mW/m ² LED_534 nm ; Ee= 155 mW/m ² | 2825 | 3766 | 4707 | counts | 4 |
| R _{e_FY} | Irradiance responsivity channel FY | LED_534 nm ; Ee= 155 mW/m ² LED_593 nm ; Ee= 155 mW/m ² | 2733 | 3644 | 4555 | counts | 4 |
| R _{e_F5} | Irradiance responsivity channel F5 | LED_531 nm ; Ee= 155 mW/m ² LED_594 nm ; Ee= 155 mW/m ² | 1197 | 1595 | 1993 | counts | 4 |
| R _{e_FXL} | Irradiance responsivity channel FXL | LED_593 nm ; Ee= 155 mW/m ² LED_628 nm ; Ee= 155 mW/m ² | 3537 | 4715 | 5893 | counts | 4 |
| R _{e_F6} | Irradiance responsivity channel F6 | LED_618 nm ; Ee= 155 mW/m ² LED_665 nm ; Ee= 155 mW/m ² | 2484 | 3311 | 4138 | counts | 4 |
| R _{e_F7} | Irradiance responsivity channel F7 | LED_685 nm ; Ee= 155 mW/m ² LED_715 nm ; Ee= 155 mW/m ² | 3819 | 5092 | 6365 | counts | 4 |
| R _{e_F8} | Irradiance responsivity channel F8 | LED_715 nm ; Ee= 155 mW/m ² LED_766 nm ; Ee= 155 mW/m ² | 468 | 930 | 1392 | counts | 4 |
| R _{e_NIR} | Irradiance responsivity channel NIR | LED_849 nm ; Ee= 155 mW/m ² LED_903 nm ; Ee= 155 mW/m ² | 5486 | 7314 | 9142 | counts | 4 |
| R _{e_FD} | Irradiance responsivity channel Flicker | LED_593 nm ; Ee= 155 mW/m ² LED_766 nm ; Ee= 155 mW/m ² FD_GAIN=64x | 3048 | 4064 | 5080 | counts | 4 |
| R _{e_VIS} | Irradiance responsivity channel VIS | LED_396 nm ; Ee= 155 mW/m ² LED_766 nm ; Ee= 155 mW/m ² 2 VIS PDs read-out | 904 | 1205 | 1506 | counts | 4 |

(1) Irradiance responsivity is measured under diffused light.

(2) Repeated temperature stress during e.g. soldering may alter measurements results and optical performance.

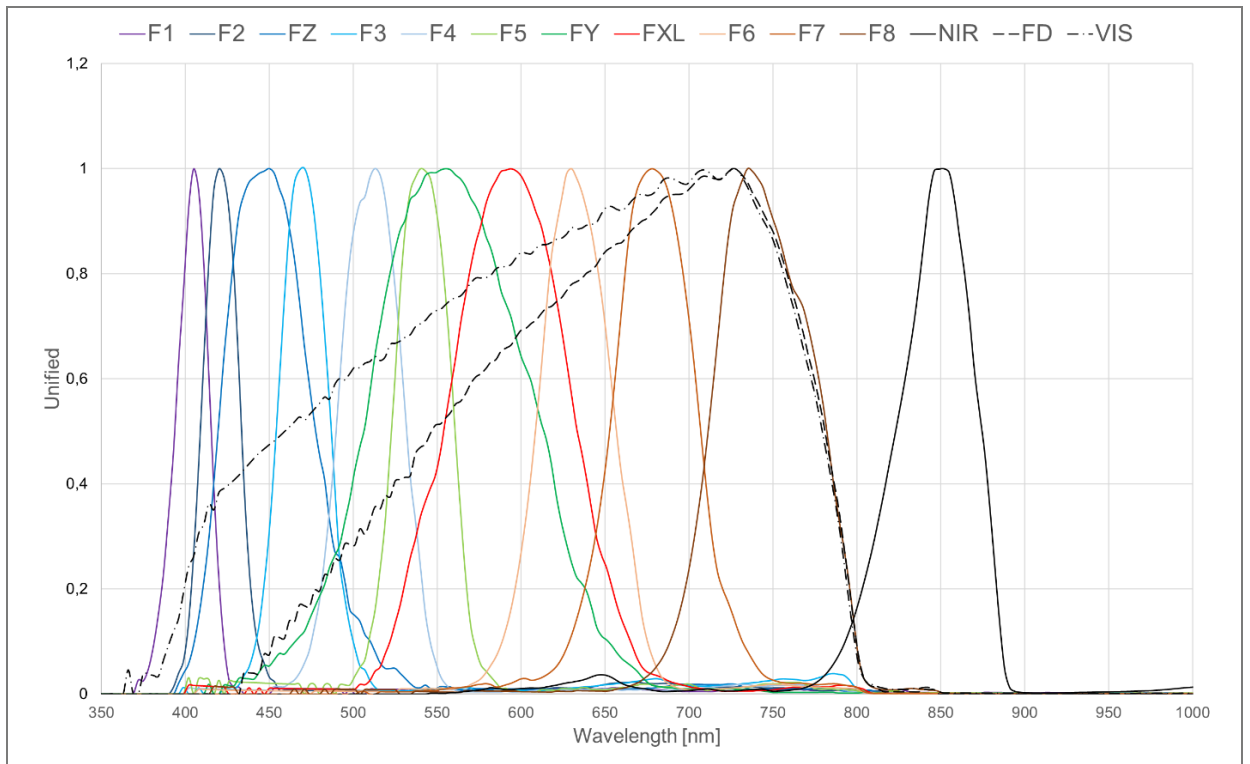
Table 7: Optical characteristics of TCS3448, AGAIN: 128x, integration time: 11 ms (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Test level |
|---------------------------|--|---|----------------------|------------------|----------------------|-------------------------|------------|
| Dark_1 ⁽²⁾ | Dark ADC count value | Ee = 0 $\mu\text{W}/\text{cm}^2$ AGAIN: 512x Integration time: 98 ms | | 0 | 5 | counts | 4 |
| Gain ratio ⁽³⁾ | Optical gain ratios, relative to 128x gain setting | AGAIN: 0.5x | 2.71 ⁽¹⁾ | 2.9 | 3.06 ⁽¹⁾ | See note ⁽⁴⁾ | 2 |
| | | AGAIN: 1x | 6.61 ⁽¹⁾ | 7.05 | 7.41 ⁽¹⁾ | | 2 |
| | | AGAIN: 2x | 14.49 ⁽¹⁾ | 15.3 | 16.11 ⁽¹⁾ | | 2 |
| | | AGAIN: 4x | 23.5 | 31.4 | 38.8 | | 4 |
| | | AGAIN: 8x | 53.4 | 61.05 | 68.4 | | 4 |
| | | AGAIN: 16x | 115.6 | 123.02 | 130.7 | | 4 |
| | | AGAIN: 32x | 1/4.16 | 1/4.04 | 1/3.89 | | 4 |
| | | AGAIN: 64x | 1/2.06 | 1/2 | 1/1.91 | | 4 |
| | | AGAIN: 128x | | 1 ⁽³⁾ | | | 4 |
| | | AGAIN: 256x | 1.91 | 2.05 | 2.19 | | 4 |
| | | AGAIN: 512x | 4.01 | 4.3 | 4.78 | | 4 |
| | | AGAIN: 1024x | 7.09 | 8.3 | 9.43 | | 4 |
| AGAIN: 2048x | 12.1 | 17.6 | 22.9 | 4 | | | |
| ADC noise ⁽⁵⁾ | | White LED, 2700K Integration time: 100 ms | | 0.05 | | % full scale | 1 |
| t _{int} | Typical integration time ⁽⁶⁾ | ASTEP = 599 ATIME = 29 | | 50 | | ms | 1 |
| t _{ASTEP} | Integration time step size | ASTEP = 999 | | 2.78 | | ms | 1 |
| h _{ca} | Half cone angle ⁽⁷⁾ | On the sensor | | 37 | | deg | 1 |

- (1) Test light irradiance of ATE too small for measurement of gain ratio variation. Variation has been measured during lab bench characterization.
- (2) The typical 3-sigma distribution is between 0 and 1 counts for AGAIN setting of 16x.
- (3) The gain ratios are relative to 128x gain setting. The ratio states the worst value measured over the 6 channels.
- (4) AGAIN ratio 0.5x to 16x is multiplied by 1000 for easier readability.
- (5) ADC noise is calculated as the standard deviation of relative to full scale.
- (6) Integration time, in milliseconds, is equal to: (ATIME + 1) x (ASTEP + 1) x 2.78 μs .
- (7) Simulated value for center photodiode.

7 Typical operating characteristics

Figure 3: Typical spectral responsivity

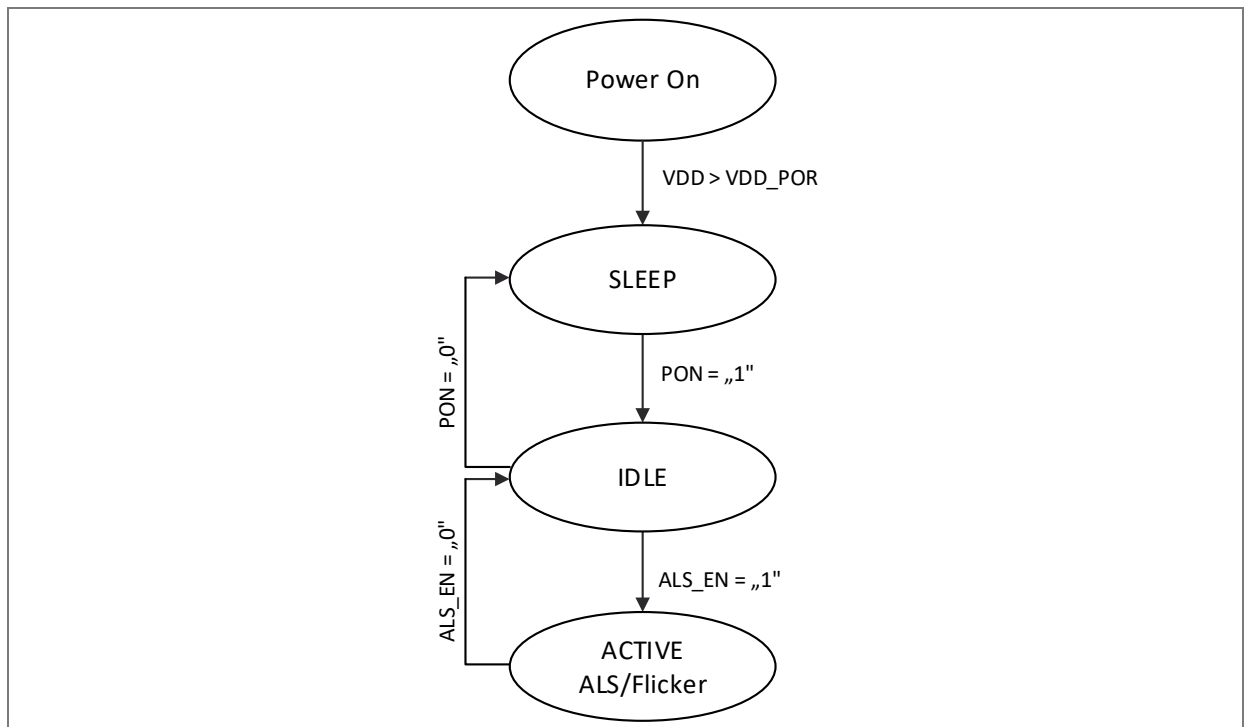


8 Functional description

Upon power-up (POR), the device initializes. During initialization (typically 200 μ s), the device will deterministically send NAK on I²C and cannot accept I²C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during this state, the I²C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the ALS measurement is enabled (ALS_EN = "1"), the device enters the ACTIVE state. If the ALS measurement is disabled (ALS_EN = "0"), the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state.

If Sleep after Interrupt is enabled (SAI = "1" in register 0xC7), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xBC and the clear status bit is in register 0xFA).

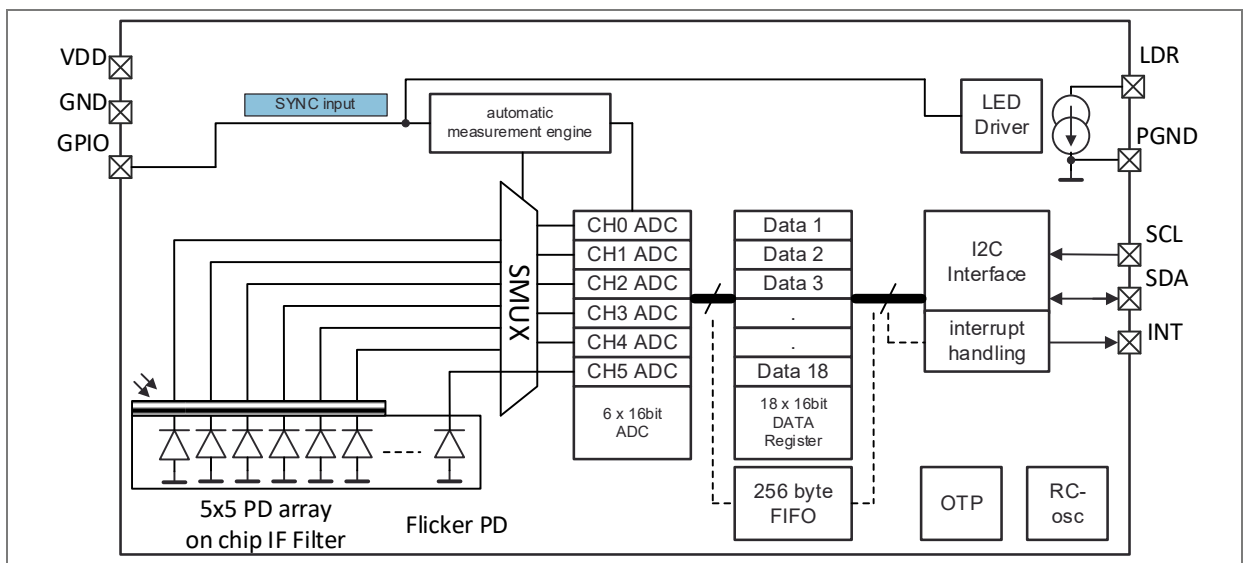
Figure 4: Simplified state diagram



8.1 Device architecture

The device features six independent 16-bit ADCs. Gain and integration time of the six ADCs can be adjusted with the I²C interface. A wait time can be programmed to automatically set a delay between two consecutive ALS measurements and to reduce overall power consumption. Once a measurement is started, the device is automatically processing the channels and storing the measurement data on chip in the corresponding data registers.

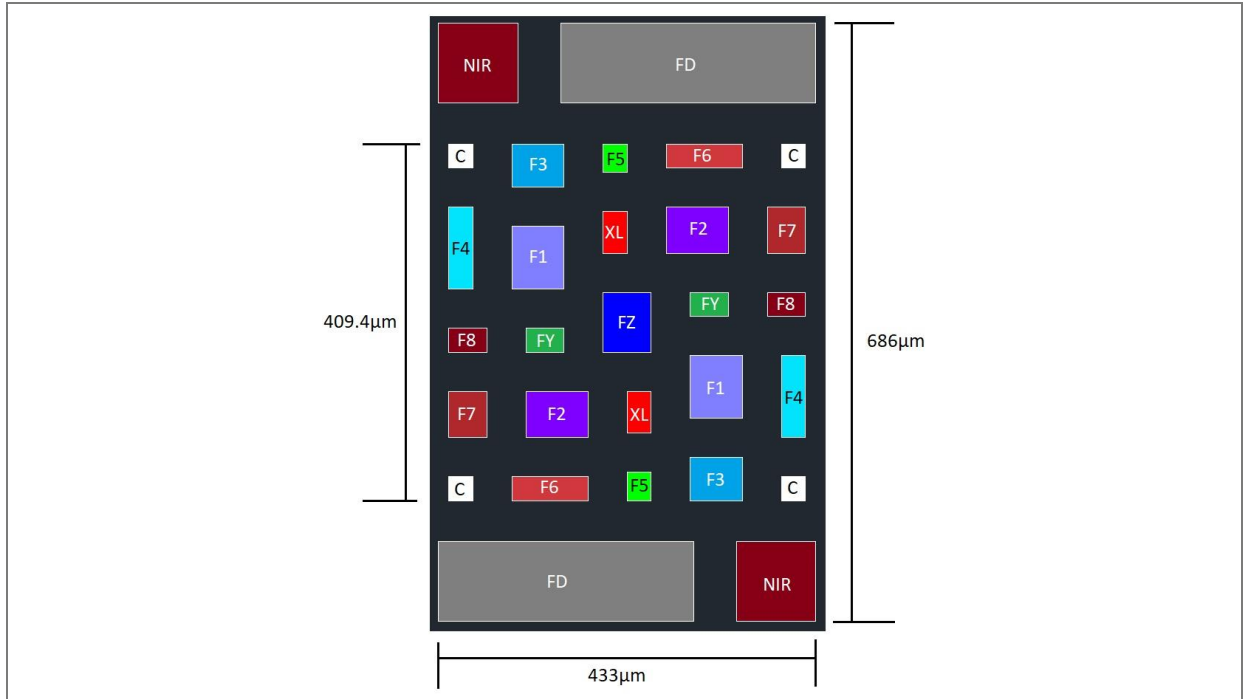
Figure 5: Simplified block diagram



8.2 Sensor array

The device features a 5 x 5-photodiode array. On top and below the photodiode array there are two photodiodes with dedicated functions such as flicker detection (“FD”) and near-infrared response (“NIR”). The photodiode “C” represents a photodiode without filter and is responsive in the visible spectral range (“VIS”).

Figure 6: Sensor array



8.3 GPIO

The GPIO can be used synchronization input to start/stop the ALS measurement. It also allows synchronizing the LED driver (LDR) with an external start/stop signal. Default state of the GPIO is “output”.

8.4 Interrupt (INT)

The interrupt (INT) can be used to define thresholds and read-out the device only when the channel threshold has been reached. The pin is active low.

8.5 LED driver (LDR)

The LED driver is programmable and can be used to drive external LEDs. It is also possible to synchronize the LED driver with an external start/stop signal via pin GPIO.

9 I²C interface

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

9.1 I²C address

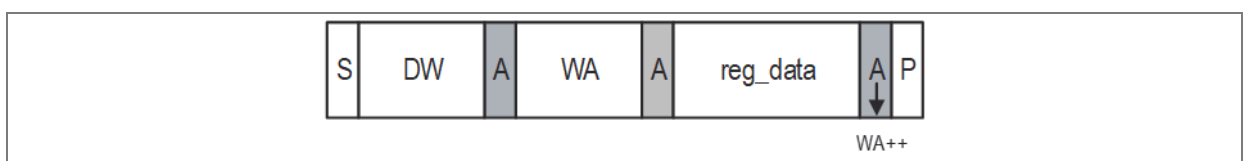
Table 8: TCS3448 I²C slave address

| Device | I ² C address |
|---------|--------------------------|
| TCS3448 | 0x59 |

9.2 I²C write transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9th clock pulse) the slave places an ACKNOWLEDGE/NOT-ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

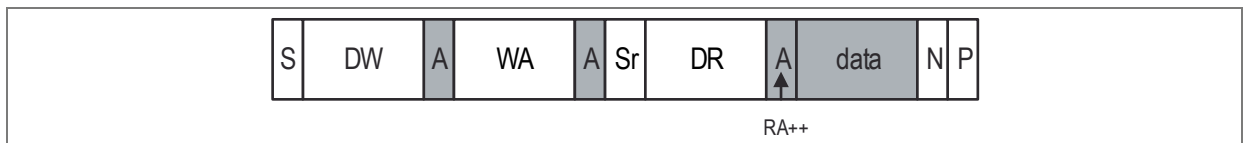
Figure 7: I²C byte write



9.3 I²C read transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Figure 8: I²C read



9.4 Timing characteristics

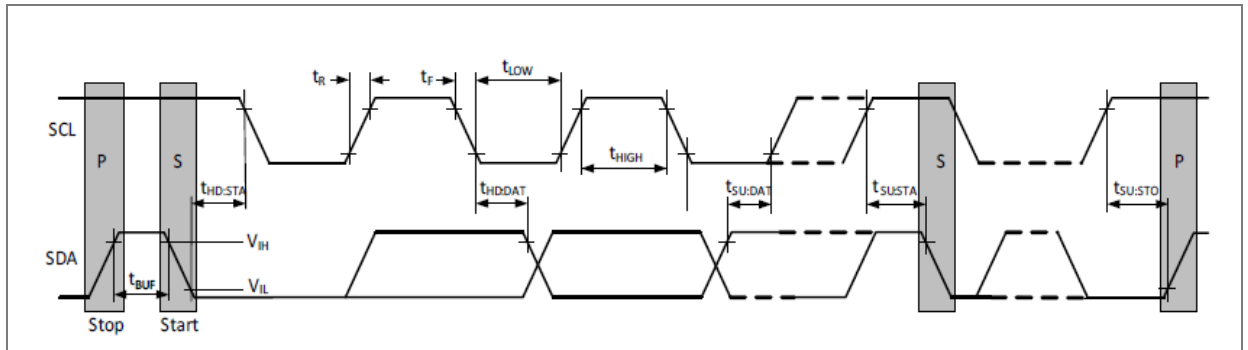
Parameters listed under Test Level 4 are guaranteed with production tests and SQC (Statistical Quality Control). Parameters listed under Test Level 3 are measured in-line with transparent monitor glasses. Parameters listed under Test Level 2 are measured in lab bench characterization. Parameters listed under Test Level 1 are guaranteed by design. All Test Levels are measured with VDD = 1.8 V and T_A = 25°C unless otherwise noted.

Table 9: I²C timing characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test level |
|---------------------|--|-----|-----|-----|------|------------|
| f _{SCL} | I ² C clock frequency | | | 1 | MHz | 4 |
| t _{BUF} | Bus free time between start and stop condition | 1.3 | | | | 1 |
| t _{HD;STA} | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 | | | μs | 1 |
| t _{SU;STA} | Repeated start condition setup time | 0.6 | | | | 1 |
| t _{SU;STO} | Stop condition setup time | 0.6 | | | | 1 |
| t _{LOW} | SCL clock low period | 1.3 | | | | 1 |
| t _{HIGH} | SCL clock high period | 0.6 | | | | 1 |
| t _{HD;DAT} | Data hold time | 0 | | | ns | 1 |
| t _{SU;DAT} | Data setup time | 100 | | | | 1 |
| t _F | Clock/data fall time | | | 300 | | 1 |
| t _R | Clock/data rise time | | | 300 | 1 | |

9.5 Timing diagrams

Figure 9: I²C slave timing diagram



9.6 Selection of I²C bus interface voltage¹

Only once, 600 μ s after startup, the voltage level at the GPIO pin will be measured. There is no I²C communication possible before 600 μ s. “Startup” is determined by a “Power on Reset” at the VDD pin.

If the voltage level at the GPIO pin is higher than 1.5 V (± 0.15 V), 1.8 V is selected as I/O voltage for SCL and SDA pins. If the voltage level at the GPIO pin lower than 1.5 V (± 0.15 V), 1.2 V is selected as I/O voltage for SCL and SDA pins.

If the GPIO pin is connected to VSS, the I/O voltage for SCL and SDA pins will always be 1.2 V.

After Startup and GPIO pin scan (which takes 600 μ s) the GPIO pin is configured as open drain I/O as known from pin-compatible earlier products.

It is NOT allowed to leave the GPIO pin floating. It shall always be connected to VSS or VBUS. VBUS is usually identical to VDD of the host processor but can also be a separate supply rail for the I²C bus.

For exact I/O voltage levels please refer to Electrical characteristics.

¹ ams OSRAM patents pending.

10 Register description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0). GRAY fields are reserved and their values must not be changed at any time.

In order to access registers from 0x58 to 0x66 bit REG_BANK in register CFG0 (0xBF) needs to be set to “1”.

10.1 Register overview

Table 10: Register overview

| Addr | Name | <D7> | <D6> | <D5> | <D4> | <D3> | <D2> | <D1> | <D0> | |
|------|----------|--------------------|------|------|------|--------------------|--------|-----------------|------|--|
| 0x58 | AUXID | | | | | | | AUXID [3:0] | | |
| 0x59 | REVID | | | | | | | REVID [2:0] | | |
| 0x5A | ID | ID [7:0] | | | | | | | | |
| 0x66 | CFG12 | | | | | | | ALS_TH_CH [2:0] | | |
| 0x80 | ENABLE | | | FDEN | | | SMUXEN | WEN | | |
| 0x81 | ATIME | ATIME [7:0] | | | | | | | | |
| 0x83 | WTIME | WTIME [7:0] | | | | | | | | |
| 0x84 | ALS_TH_L | ALS_TH_L_LSB [7:0] | | | | | | | | |
| 0x85 | | ALS_TH_L_MSB [7:0] | | | | | | | | |
| 0x86 | ALS_TH_H | ALS_TH_H_LSB [7:0] | | | | | | | | |
| 0x87 | | ALS_TH_H_MSB [7:0] | | | | | | | | |
| 0x93 | STATUS | ASAT | | | | AINT | FINT | | | |
| 0x94 | ASTATUS | ASAT_STATUS | | | | AGAIN_STATUS [3:0] | | | | |
| 0x95 | ADATA0 | ADATA0_L [7:0] | | | | | | | | |
| 0x96 | | ADATA0_H [7:0] | | | | | | | | |
| 0x97 | ADATA1 | ADATA1_L [7:0] | | | | | | | | |
| 0x98 | | ADATA1_H [7:0] | | | | | | | | |
| 0x99 | ADATA2 | ADATA2_L [7:0] | | | | | | | | |
| 0x9A | | ADATA2_H [7:0] | | | | | | | | |

| Addr | Name | <D7> | <D6> | <D5> | <D4> | <D3> | <D2> | <D1> | <D0> |
|------|----------|-------------|--------|---------------|-----------------|--------------|----------------|---------------|---------------|
| 0x9B | ADATA3 | | | | ADATA3_L [7:0] | | | | |
| 0x9C | | | | | ADATA3_H [7:0] | | | | |
| 0x9D | ADATA4 | | | | ADATA4_L [7:0] | | | | |
| 0x9E | | | | | ADATA4_H [7:0] | | | | |
| 0x9F | ADATA5 | | | | ADATA5_L [7:0] | | | | |
| 0xA0 | | | | | ADATA5_H [7:0] | | | | |
| 0xA1 | ADATA6 | | | | ADATA6_L [7:0] | | | | |
| 0xA2 | | | | | ADATA6_H [7:0] | | | | |
| 0xA3 | ADATA7 | | | | ADATA7_L [7:0] | | | | |
| 0xA4 | | | | | ADATA7_H [7:0] | | | | |
| 0xA5 | ADATA8 | | | | ADATA8_L [7:0] | | | | |
| 0xA6 | | | | | ADATA8_H [7:0] | | | | |
| 0xA7 | ADATA9 | | | | ADATA9_L [7:0] | | | | |
| 0xA8 | | | | | ADATA9_H [7:0] | | | | |
| 0xA9 | ADATA10 | | | | ADATA10_L [7:0] | | | | |
| 0xAA | | | | | ADATA10_H [7:0] | | | | |
| 0xAB | ADATA11 | | | | ADATA11_L [7:0] | | | | |
| 0xAC | | | | | ADATA11_H [7:0] | | | | |
| 0xAD | ADATA12 | | | | ADATA12_L [7:0] | | | | |
| 0xAE | | | | | ADATA12_H [7:0] | | | | |
| 0xAF | ADATA13 | | | | ADATA13_L [7:0] | | | | |
| 0xB0 | | | | | ADATA13_H [7:0] | | | | |
| 0xB1 | ADATA14 | | | | ADATA14_L [7:0] | | | | |
| 0xB2 | | | | | ADATA14_H [7:0] | | | | |
| 0xB3 | ADATA15 | | | | ADATA15_L [7:0] | | | | |
| 0xB4 | | | | | ADATA15_H [7:0] | | | | |
| 0xB5 | ADATA16 | | | | ADATA16_L [7:0] | | | | |
| 0xB6 | | | | | ADATA16_H [7:0] | | | | |
| 0xB7 | ADATA17 | | | | ADATA17_L [7:0] | | | | |
| 0xB8 | | | | | ADATA17_H [7:0] | | | | |
| 0x90 | STATUS 2 | | AVALID | | ASAT_ DIG | ASAT_ ANA | | FDSAT_ ANA | FDSAT_ DIG |
| 0x91 | STATUS 3 | | | INT_ALS_H | INT_AL S_L | | | | |
| 0xBB | STATUS 5 | | | | | SINT_ _FD | SINT_ _SMUX | | |
| 0xBC | STATUS 4 | FIFO_ OV | | OVTEMP | FD_TRI G | | ALS_TRI G | SAL_ ACT | INT_BUS Y |
| 0xBF | CFG 0 | | | LOW_ POWER | REG_ BANK | | WLONG | | |

| Addr | Name | <D7> | <D6> | <D5> | <D4> | <D3> | <D2> | <D1> | <D0> | |
|------|-----------|------------------------|---|-----------------|-------|----------------|-----------|---------------|---------|--|
| 0xC6 | CFG1 | | | | | AGAIN[4:0] | | | | |
| 0xC7 | CFG3 | | | | SAI | | | | | |
| 0xF5 | CFG6 | | | | SMUX_ | | CMD [4:3] | | | |
| 0xC9 | CFG8 | FIFO_TH [7:6] | | | | | | | | |
| 0xCA | CFG9 | | SIEN_ | | SIEN_ | | | | | |
| | | | FD | | SMUX | | | | | |
| 0x65 | CFG10 | | | | | | | FD_PERS [2:0] | | |
| 0xCF | PERS | | | | | APERS [3:0] | | | | |
| 0x6B | GPIO | | | | | GPIO_ | GPIO_ | GPIO_ | GPIO_ | |
| | | | | | | INV | IN_EN | OUT | IN | |
| 0xD4 | ASTEP | ASTEP [7:0] | | | | | | | | |
| 0xD5 | | ASTEP [15:8] | | | | | | | | |
| 0xD6 | CFG20 | FD_FIF | auto_SMUX | | | | | | | |
| | | O_8b | | | | | | | | |
| 0xCD | LED | LED_AC | | LED_DRIVE [6:0] | | | | | | |
| | | T | | | | | | | | |
| 0xD7 | AGC_GAIN_ | AGC_FD_GAIN_MAX [7:4] | | | | | | | | |
| | MAX | | | | | | | | | |
| 0xDE | AZ_CONFIG | AT_NTH_ITERATION [7:0] | | | | | | | | |
| 0xE0 | FD_TIME_1 | FD_TIME [7:0] | | | | | | | | |
| 0xE2 | FD_TIME_2 | FD_GAIN [7:3] | | | | FD_TIME [10:8] | | | | |
| 0xDF | FD_CFG0 | FIFO_W | | | | | | | | |
| | | RITE_F | | | | | | | | |
| | | D | | | | | | | | |
| 0xE3 | FD_STATUS | | | FD_ | FD_ | FD_ | FD_ | FD_ | FD_ | |
| | | | | VALID | SAT | 120Hz_ | 100Hz_ | 120Hz | 100Hz | |
| | | | | | | VALID | VALID | | | |
| 0xF9 | INTENAB | ASIEN | | | | ALS_IEN | FIEN | | SIEN | |
| 0xFA | CONTROL | | | | | SW_ | ALS_MA | FIFO_ | CLEAR_ | |
| | | | | | | RESET | N_AZ | CLR | SAI_ACT | |
| 0xFC | FIFO_MAP | | FIFO_WRITE_CH5_DATA – FIFO_WRITE_CH0_DATA [6:1] | | | | | | ASTATU | |
| | | | | | | | | | S | |
| 0xFD | FIFO_LVL | FIFO_LVL [7:0] | | | | | | | | |
| 0xFE | FDATA | FDATA_L [7:0] | | | | | | | | |
| 0xFF | | FDATA_H [15:8] | | | | | | | | |

10.2 Detailed register description

For easier readability, the detailed register description is done in groups of registers related to dedicated device functions. This is not necessarily related to its register address.

Explanation of register access abbreviations:

RW = Read or write

R = Read only

W = Write only

SC = Self-clearing after access

10.2.1 Enable and configuration registers

Table 11: ENABLE register

| Addr: 0x80 | | ENABLE | | |
|------------|----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | Reserved | 0 | RW | Reserved |
| 6 | FDEN | 0 | RW | Flicker Detection Enable. 0: Flicker Detection disabled. 1: Flicker Detection enabled. |
| 5 | Reserved | 0 | RW | Reserved |
| 4 | SMUXEN | 0 | RW | SMUX Enable. 1: Starts SMUX command. Note: This bit gets cleared automatically as soon as SMUX operation is finished. |
| 3 | WEN | 0 | RW | Wait Enable. 0: Wait time between two consecutive ALS measurements disabled. 1: Wait time between two consecutive ALS measurements enabled. |
| 2 | Reserved | 0 | RW | Reserved |
| 1 | ALS_EN | 0 | RW | ALS Measurement Enable. 0: ALS measurement disabled. 1: ALS measurement enabled. |
| 0 | PON | 0 | RW | Power ON. 0: TCS3448 disabled. 1: TCS3448 enabled. Note: When bit is set, internal oscillator is activated, allowing timers and ADC channels to operate. |

10.2.1.1 GPIO register (Address 0x6B)

Table 12: GPIO register

| Addr: 0x6B | | GPIO | | |
|------------|------------|---------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:4 | Reserved | 0 | | Reserved |
| 3 | GPIO_INV | 0 | RW | GPIO Invert. If set, the GPIO output is inverted. |
| 2 | GPIO_IN_EN | 0 | RW | GPIO Input Enable. If set, the GPIO pin accepts a non-floating input. |
| 1 | GPIO_OUT | 1 | RW | GPIO Output. If set, the output state of the GPIO is active directly. |
| 0 | GPIO_IN | 0 | R | GPIO Input. Indicates the status of the GPIO input if GPIO_IN_EN is set. |

10.2.1.2 LED register (Address 0xCD)

Table 13: LED register

| Addr: 0xCD | | LED | | |
|------------|-----------|----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7 | LED_ACT | 0 | RW | LED Control. 0: External LED connected to pin LDR off. 1: External LED connected to pin LDR on. |
| 6:0 | LED_DRIVE | 000 0100 | RW | LED Driving Strength. 000 0000: 4 mA 000 0001: 6 mA 000 0010: 8 mA 000 0011: 10 mA 000 0100: 12 mA 111 1110: 256 mA 111 1111: 258 mA |

10.2.1.3 INTENAB register (Address 0xF9)

Table 14: INTENAB register

| Addr: 0xF9 | | INTENAB | | |
|------------|----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | ASIEN | 0 | RW | ALS and Flicker Detect Saturation Interrupt Enable. When asserted permits saturation interrupts to be generated. |
| 6:4 | Reserved | | | Reserved |
| 3 | ALS_IEN | 0 | RW | ALS Interrupt Enable. When asserted permits interrupts to be generated, subject to the ALS thresholds and persistence filter. Bit is mirrored in the ENABLE register. |
| 2 | F_IEN | 0 | RW | FIFO Buffer Interrupt Enable. When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition. |
| 1 | Reserved | 0 | | Reserved |
| 0 | SIEN | | RW | System Interrupt Enable. When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed or SMUX operation has finished. |

10.2.1.4 CONTROL register (Address 0xFA)

Table 15: CONTROL register

| Addr: 0xFA | | CONTROL | | |
|------------|---------------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:4 | Reserved | 0 | | Reserved |
| 3 | SW_RESET | 0 | RW | Software Reset When set the device will force a power on reset. |
| 2 | ALS_MAN_AZ | 0 | RW | ALS Engine Manual Autozero. Starts a manual autozero of the ALS engines. Set ALS_EN = 0 before starting a manual autozero for it to work. |
| 1 | FIFO_CLR | 0 | RW | FIFO Buffer Clear. Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL. |
| 0 | CLEAR_SAI_ACT | 0 | RW | Clear Sleep-After-Interrupt Active. Clears SAI_ACTIVE, ends sleep, and restarts device operation. |

10.2.2 ADC timing configuration / integration time

The integration time is set using the ATIME (0x81) and ASTEP (0xD4, 0xD5) registers. The integration time, in milliseconds, is equal to:

Equation 1: Setting the integration time

$$t_{int} = (ATIME + 1) \times (ASTE P + 1) \times 2.78 \mu s$$

It is not allowed that both settings –ATIME and ASTEP – are set to “0”.

The integration time also defines the full-scale ADC value, which is equal to:

Equation 2: ADC full scale value²

$$ADC_{fullscale} = (ATIME + 1) \times (ASTE P + 1)$$

10.2.2.1 ATIME register (Address 0x81)

Table 16: ATIME register

| Addr: 0x81 | | ATIME | | | |
|------------|----------|---------|--------|---|-------------------------|
| Bit | Bit name | Default | Access | Bit description | |
| 7:0 | ATIME | 0x00 | RW | Integration Time. Sets the number of integration steps from 1 to 255. | |
| | | | | Value | Integration Time |
| | | | | 0 | ASTE P |
| | | | | n | ASTE P x (n+1) |
| | | | | 255 | ASTE P x 256 |

² The maximum ADC count is 65535. Any ATIME/ASTE P field setting resulting in higher ADC full-scale values would result in a full-scale of 65535.

10.2.2.2 ASTEP register (Address 0xD4, 0xD5)

Table 17: ASTEP register

| Addr: 0xD4, 0xD5 | | ASTEPA | | | | | | | | | | | | | | | | | | |
|------------------|-----------------------|---------|--------|---|-------|-----------|------------|--------------|---|----------------------|--------------|---------|--------------|------------------|----------------|-------|-----------------|--------|-----------------|-----------------------|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | | | | | | | |
| 7:0 0xD4 | ASTEPA LOW | 0xE7 | RW | Integration Time Step Size. Sets the integration time per step in increments of 2.78 μ s. The default value is 999 (0x03E7). | | | | | | | | | | | | | | | | |
| | ASTEPA HIGH | | | | | | | | | | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>VALUE</th> <th>STEP SIZE</th> </tr> </thead> <tbody> <tr> <td>0 (0x0000)</td> <td>2.78 μs</td> </tr> <tr> <td>n</td> <td>2.78 μs x (n+1)</td> </tr> <tr> <td>599 (0x0257)</td> <td>1.67 ms</td> </tr> <tr> <td>999 (0x03E7)</td> <td>2.78 ms(default)</td> </tr> <tr> <td>17999 (0x464F)</td> <td>50 ms</td> </tr> <tr> <td>65534 (0xFFFFE)</td> <td>182 ms</td> </tr> <tr> <td>65535 (0xFFFFE)</td> <td>Reserved, do not use.</td> </tr> </tbody> </table> | VALUE | STEP SIZE | 0 (0x0000) | 2.78 μ s | n | 2.78 μ s x (n+1) | 599 (0x0257) | 1.67 ms | 999 (0x03E7) | 2.78 ms(default) | 17999 (0x464F) | 50 ms | 65534 (0xFFFFE) | 182 ms | 65535 (0xFFFFE) | Reserved, do not use. |
| VALUE | STEP SIZE | | | | | | | | | | | | | | | | | | | |
| 0 (0x0000) | 2.78 μ s | | | | | | | | | | | | | | | | | | | |
| n | 2.78 μ s x (n+1) | | | | | | | | | | | | | | | | | | | |
| 599 (0x0257) | 1.67 ms | | | | | | | | | | | | | | | | | | | |
| 999 (0x03E7) | 2.78 ms(default) | | | | | | | | | | | | | | | | | | | |
| 17999 (0x464F) | 50 ms | | | | | | | | | | | | | | | | | | | |
| 65534 (0xFFFFE) | 182 ms | | | | | | | | | | | | | | | | | | | |
| 65535 (0xFFFFE) | Reserved, do not use. | | | | | | | | | | | | | | | | | | | |
| 15:8 0xD5 | ASTEPA HIGH | 0x03 | | | | | | | | | | | | | | | | | | |

10.2.2.3 WTIME register (Address 0x83)

If wait is enabled (WEN = “1” register 0x80), each new measurement is started based on WTIME. It is necessary for WTIME to be sufficiently long for ALS integration and any other functions to be completed within the period. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then ALS_TRIG in register STATUS6 (ADDR: 0xBC) will be set to “1”.

Table 18: WTIME register

| Addr: 0x83 | | WTIME | | | | | | | | | | | | | | | | | |
|------------|----------|-----------------|--------|---|-------------|-------------|-----------|------|---|---------|------|---|---------|---|---|-----------------|------|-----|--------|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | | | | | | |
| 7:0 | WTIME | 0x00 | RW | ALS Measurement Wait Time. 8-bit value to specify the delay between two consecutive ALS measurements. | | | | | | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>Value</th> <th>Wait Cycles</th> <th>Wait Time</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>1</td> <td>2.78 ms</td> </tr> <tr> <td>0x01</td> <td>2</td> <td>5.56 ms</td> </tr> <tr> <td>n</td> <td>n</td> <td>2.78 ms x (n+1)</td> </tr> <tr> <td>0xff</td> <td>256</td> <td>711 ms</td> </tr> </tbody> </table> | Value | Wait Cycles | Wait Time | 0x00 | 1 | 2.78 ms | 0x01 | 2 | 5.56 ms | n | n | 2.78 ms x (n+1) | 0xff | 256 | 711 ms |
| | | | | Value | Wait Cycles | Wait Time | | | | | | | | | | | | | |
| | | | | 0x00 | 1 | 2.78 ms | | | | | | | | | | | | | |
| | | | | 0x01 | 2 | 5.56 ms | | | | | | | | | | | | | |
| n | n | 2.78 ms x (n+1) | | | | | | | | | | | | | | | | | |
| 0xff | 256 | 711 ms | | | | | | | | | | | | | | | | | |
| 0x00 | 1 | 2.78 ms | | | | | | | | | | | | | | | | | |
| 0x01 | 2 | 5.56 ms | | | | | | | | | | | | | | | | | |
| n | n | 2.78 ms x (n+1) | | | | | | | | | | | | | | | | | |
| 0xff | 256 | 711 ms | | | | | | | | | | | | | | | | | |

10.2.2.4 FD_TIME register (Address 0xE0, 0xE2)

The register FD_Time_1 and FD_Time_2 can be used to configure the integration time and gain (ADC 5) of the flicker detection independently from the other ADCs. The FD_TIME register is an 11-bit register with the MSB in register 0xDA (bit 10:8) and the LSB in register 0xD8 (bit 7:0). The bit FDEN (register 0x80) must be set to “1” in order to use the FD_TIME registers. If the bit FDEN is not set, ADC5 runs automatically with the same gain and integration time as ADC0 to ADC4.

Equation 3: Calculating the flicker detection integration time

$$t_{int_FD} = FD_TIME \times 2.78 \mu s$$

Table 19: FD_Time_1 register

| Addr: 0xE0 | | FD_TIME_1 | | |
|------------|---------------|-----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | FD_TIME [7:0] | 0110 0111 | RW | LSB of flicker detection integration time. Note: Must not be changed during FDEN = 1 and PON = 1. |

Table 20: FD_Time_2 register

| Addr: 0xE2 | | FD_TIME_2 | | |
|--|----------------|-----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| Flicker Detection Gain Setting (ADC5) | | | | |
| VALUE | | | | |
| GAIN | | | | |
| | | | | 0 |
| | | | | 0.5x |
| | | | | 1 |
| | | | | 1x |
| | | | | 2 |
| | | | | 2x |
| | | | | 3 |
| | | | | 4x |
| | | | | 4 |
| | | | | 8x |
| 7:3 | FD_GAIN | 9 | RW | 5 |
| | | | | 16x |
| | | | | 6 |
| | | | | 32x |
| | | | | 7 |
| | | | | 64x |
| | | | | 8 |
| | | | | 128x |
| | | | | 9 |
| | | | | 256x |
| | | | | 10 |
| | | | | 512x |
| | | | | 11 |
| | | | | 1024x |
| | | | | 12 |
| | | | | 2048x |
| 2:0 | FD_TIME [10:8] | 1 | RW | MSB of flicker detection integration time. Note: Must not be changed during FDEN = 1 and PON = 1. |

10.2.3 ADC configuration

The following registers provide configuration for the 6 integrated ADCs (CH0 to CH5). It is possible to adjust the gain and setup the auto zero compensation for the ADCs.

10.2.3.1 CFG1 register (Address 0xC6)

Table 21: CFG1 register

| Addr: 0xC6 | | CFG1 | | |
|------------|----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:5 | Reserved | 0 | | Reserved |
| | | | | ALS Engines Gain Setting. Sets the ALS sensitivity. |
| | | | | VALUE GAIN |
| | | | | 0 0.5x |
| | | | | 1 1x |
| | | | | 2 2x |
| | | | | 3 4x |
| | | | | 4 8x |
| 4:0 | AGAIN | 9 | RW | 5 16x |
| | | | | 6 32x |
| | | | | 7 64x |
| | | | | 8 128x |
| | | | | 9 256x |
| | | | | 10 512x |
| | | | | 11 1024x |
| | | | | 12 2048x |

10.2.3.2 CFG10 register (Address 0x65)

Table 22: CFG10 register

| Addr: 0x65 | | CFG10 | | |
|------------|----------|----------|----------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:3 | Reserved | Reserved | Reserved | Reserved |
| 2:0 | FD_PERS | 2 | RW | <p>Flicker Detect Persistence. Sets the number of consecutive flicker detect results that must be different before the flicker detect status will be changed. Flicker detection interrupts on SINT are affected by this setting. Flicker detect persistence is equal to $2^{(FD_PERS-1)}$ Setting "0" equals to every time.</p> |

10.2.3.3 AZ_CONFIG register (Address 0xDE)

The following register configures how often the ALS engine offsets are reset (auto zero) to compensate for changes of the device temperature. The typical time auto zero needs to be completed is 15 ms.

Table 23: AZ_CONFIG register

| Addr: 0xDE | | AZ_CONFIG | | | | | | | | | | | | | | | | |
|------------|-------------------------------------|-----------|--------|---|-------|--------------------|---|-------------------------|---|-------------------------|---|----------------|-----|--------------------------------|-----|------------------|-----|-------------------------------------|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | | | | | |
| 7:0 | AZ_NTH_ITERATION | 255 | RW | <p>AUTOZERO FREQUENCY. Sets the frequency at which the device performs auto zero of the ALS engines. Note: If FDEN = "1" auto zero is also done for ADC 5. The flicker detection measurement will be interrupted and restarted in this case.</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>AUTOZERO FREQUENCY</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Never (not recommended)</td> </tr> <tr> <td>1</td> <td>Every integration cycle</td> </tr> <tr> <td>2</td> <td>Every 2 cycles</td> </tr> <tr> <td>...</td> <td>Every "AZ_NTH_ITERATION" cycle</td> </tr> <tr> <td>254</td> <td>Every 254 cycles</td> </tr> <tr> <td>255</td> <td>Only before first measurement cycle</td> </tr> </tbody> </table> | VALUE | AUTOZERO FREQUENCY | 0 | Never (not recommended) | 1 | Every integration cycle | 2 | Every 2 cycles | ... | Every "AZ_NTH_ITERATION" cycle | 254 | Every 254 cycles | 255 | Only before first measurement cycle |
| VALUE | AUTOZERO FREQUENCY | | | | | | | | | | | | | | | | | |
| 0 | Never (not recommended) | | | | | | | | | | | | | | | | | |
| 1 | Every integration cycle | | | | | | | | | | | | | | | | | |
| 2 | Every 2 cycles | | | | | | | | | | | | | | | | | |
| ... | Every "AZ_NTH_ITERATION" cycle | | | | | | | | | | | | | | | | | |
| 254 | Every 254 cycles | | | | | | | | | | | | | | | | | |
| 255 | Only before first measurement cycle | | | | | | | | | | | | | | | | | |

10.2.3.4 AGC_GAIN_MAX register (Address 0xD7)

Table 24: AGC_GAIN_MAX register

| Addr: 0xD7 | | AGC_GAIN_MAX | | |
|------------|-----------------|--------------|----------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:4 | AGC_FD_GAIN_MAX | 9 | RW | <p>Flicker Detection AGC Gain Max. Sets the maximum gain for flicker detection to $2^{AGC_FD_GAIN_MAX}$. Default value is 9 (256x). The range can be set from 0 (0.5x) to 10 (2048x).</p> |
| 3:0 | Reserved | 9 | Reserved | Reserved |

10.2.3.5 CFG8 register (Address 0xC9)

Table 25: CFG8 register

| Addr: 0xC9 | | CFG8 | | | | | | | | | | | | |
|------------|----------|---------|--------|---|-------|----------|---|---|---|---|---|---|---|----|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | |
| 7:6 | FIFO_TH | 2 | RW | <p>FIFO Threshold. Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT).</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>FIFO_LVL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>16</td> </tr> </tbody> </table> | VALUE | FIFO_LVL | 0 | 1 | 1 | 4 | 2 | 8 | 3 | 16 |
| VALUE | FIFO_LVL | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | |
| 1 | 4 | | | | | | | | | | | | | |
| 2 | 8 | | | | | | | | | | | | | |
| 3 | 16 | | | | | | | | | | | | | |
| 5:0 | Reserved | 0 | | Reserved | | | | | | | | | | |

10.2.4 Device identification

The following registers provided device identification. Device ID, revision ID and auxiliary ID are read only.

10.2.4.1 AUXID register (Address 0x58)

Table 26: AUXID register

| Addr: 0x58 | | AUXID | | |
|------------|----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:4 | Reserved | | | Reserved |
| 3:0 | AUXID | 0000 | R | Auxiliary Identification TCS3448 |

10.2.4.2 REVID register (Address 0x59)

Table 27: REVID register

| Addr: 0x59 | | REVID | | |
|------------|----------|---------|--------|---------------------------------------|
| Bit | Bit name | Default | Access | Bit description |
| 7:3 | Reserved | | | Reserved |
| 2:0 | REV_ID | 000 | R | Revision Number Identification |

10.2.4.3 ID register (Address 0x5A)

Table 28: ID register

| Addr: 0x5A | | ID | | |
|------------|----------|----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | ID | 10000001 | R | Part Number Identification Value 10000001 |

10.2.5 ALS interrupt configuration

The ALS interrupt threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CH0_DATA values (ADC CH0). If ALS_IEN (register 0xF9) is enabled and CH0_DATA is not between the two thresholds for the number of consecutive measurements specified in APERS (register 0xBD) an interrupt is set.

10.2.5.1 ALS_TH_L_LSB register (Address 0x84)

Table 29: ALS_TH_L_LSB register

| Addr: 0x84 | | ALS_TH_L_LSB | | |
|------------|--------------|--------------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | ALS_TH_L_LSB | 0x00 | RW | ALS Low Threshold LSB This register provides the low byte of the low interrupt threshold (CH0). |

10.2.5.2 ALS_TH_L_MSB register (Address 0x85)

Table 30: ALS_TH_L_MSB register

| Addr: 0x85 | | ALS_TH_L_MSB | | |
|------------|--------------|--------------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | ALS_TH_L_MSB | 0x00 | RW | ALS Low Threshold MSB This register provides the high byte of the low interrupt threshold (CH0). Both ALS_TH_L registers are combined to a 16-bit threshold. If the value captured by channel 0 is below the low threshold and the APERS value is reached the bit ALS_IEN is set and an interrupt is generated. There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied at the same time to avoid an invalid threshold. Note: The LSB register cannot be changed without writing to the MSB register. It is recommended to write to ALS_TH_L_LSB and ALS_TH_L_MSB within one I ² C command. |

10.2.5.3 ALS_TH_H_LSB Register (Address 0x86)

Table 31: ALS_TH_H_LSB register

| Addr: 0x86 | | ALS_TH_H_LSB | | |
|------------|--------------|--------------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | ALS_TH_H_LSB | 0x00 | RW | ALS High Threshold LSB This register provides the low byte of the high interrupt threshold (CH0). |

10.2.5.4 ALS_TH_H_MSB register (Address 0x87)

Table 32: ALS_TH_H_MSB register

| Addr: 0x87 | | ALS_TH_H_MSB | | |
|------------|--------------|--------------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | ALS_TH_H_MSB | 0x00 | RW | ALS High Threshold MSB This register provides the high byte of the high interrupt threshold (CH0). Both ALS_TH_H registers are combined to a 16-bit threshold. If the value captured by channel 0 is above the high threshold and the APERS value is reached the bit ALS_IEN is set and an interrupt is generated. |

10.2.5.5 CFG12 register (Address 0x66)

Table 33: CFG12 register

| Addr: 0x66 | | CFG12 | | | | | | | | | | | | | | | | |
|------------|-----------|---------|--------|--|-------|---------|---|-----|---|-----|---|-----|---|-----|---|-----|---|-----|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | | | | | |
| 7:3 | Reserved | 0 | | Reserved | | | | | | | | | | | | | | |
| | | | | ALS Threshold Channel. Sets the channel used for interrupts and persistence, if enabled, to determine device status and gain settings. | | | | | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>VALUE</th> <th>CHANNEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CH0</td> </tr> <tr> <td>1</td> <td>CH1</td> </tr> <tr> <td>2</td> <td>CH2</td> </tr> <tr> <td>3</td> <td>CH3</td> </tr> <tr> <td>4</td> <td>CH4</td> </tr> <tr> <td>5</td> <td>CH5</td> </tr> </tbody> </table> | VALUE | CHANNEL | 0 | CH0 | 1 | CH1 | 2 | CH2 | 3 | CH3 | 4 | CH4 | 5 | CH5 |
| VALUE | CHANNEL | | | | | | | | | | | | | | | | | |
| 0 | CH0 | | | | | | | | | | | | | | | | | |
| 1 | CH1 | | | | | | | | | | | | | | | | | |
| 2 | CH2 | | | | | | | | | | | | | | | | | |
| 3 | CH3 | | | | | | | | | | | | | | | | | |
| 4 | CH4 | | | | | | | | | | | | | | | | | |
| 5 | CH5 | | | | | | | | | | | | | | | | | |
| 2:0 | ALS_TH_CH | 0 | RW | | | | | | | | | | | | | | | |

10.2.6 Device status registers

The following registers provide status of the device and indicate details about saturation, interrupts, over temperature, device execution and ambient light flicker detection.

10.2.6.1 STATUS register (Address 0x93)

The primary status register for TCS3448 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a “1” to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s) and then write the register value back to STATUS to clear the handled events. Writing “0” will not clear those bits if they have a value of “1”, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared. In case channel saturation has happened (ASAT or FDSAT) it is recommended to discard the measurement results and re-configure device configuration such as AGAIN and Integration Time to avoid saturation.

Table 34: STATUS register

| Addr: 0x93 | | STATUS | | |
|------------|----------|---------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7 | ASAT | 0 | R, SC | ALS and Flicker Detect Saturation. If ASIEN is set, indicates ALS saturation. Check STATUS2 register to distinguish between analog or digital saturation. |
| 6:4 | Reserved | 0 | R | Reserved |
| 3 | AINT | 0 | R, SC | ALS Channel Interrupt. If ALS_IEN is set, indicates that a ALS event that met the programmed thresholds and persistence (APERS) occurred. |
| 2 | FINT | 0 | R, SC | FIFO Buffer Interrupt. If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer. |
| 1 | Reserved | 0 | R | Reserved |
| 0 | SINT | 0 | R, SC | System Interrupt. If SIEN is set, indicates that system interrupt is set. Refer to Status5 register. |

10.2.6.2 STATUS 2 register (Address 0x90)

Table 35: STATUS 2 register

| Addr: 0x90 | | STATUS 2 | | |
|------------|---------------|----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7 | Reserved | 0 | | Reserved |
| 6 | AVALID | 0 | R | ALS Valid. Indicates that the ALS measurement has been completed. |
| 5 | Reserved | 0 | | Reserved |
| 4 | ASAT_DIGITAL | 0 | R | Digital Saturation. Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register. |
| 3 | ASAT_ANALOG | 0 | R | Analog Saturation. Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit. |
| 2 | Reserved | 0 | R | Reserved |
| 1 | FDSAT_ANALOG | 0 | R | Flicker Detect Analog Saturation. Indicates that the intensity of ambient light has exceeded the maximum integration level for the analog circuit for flicker detection. |
| 0 | FDSAT_DIGITAL | 0 | R | Flicker Detect Digital Saturation. Indicates that the maximum counter value has been reached during flicker detection. |

10.2.6.3 STATUS 3 register (Address 0x91)

Table 36: STATUS 3 register

| Addr: 0x91 | | STATUS 3 | | |
|------------|-----------|----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:6 | Reserved | 0 | | Reserved |
| 5 | INT_ALS_H | 0 | R | ALS Interrupt High. Indicates that a ALS interrupt occurred because the data exceeded the high threshold. |
| 4 | INT_ALS_L | 0 | R | ALS Interrupt Low. Indicates that a ALS interrupt occurred because the data is below the low threshold. |
| 3:0 | Reserved | 0 | | Reserved |

10.2.6.4 STATUS 5 register (Address 0xBB)

Table 37: STATUS 5 register

| Addr: 0xBB | | STATUS 5 | | |
|------------|-----------|----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:4 | Reserved | 0 | | Reserved |
| 3 | SINT_FD | 0 | R | Flicker Detect Interrupt. If SIEN_FD is set, indicates that the FD_STATUS register status has changed. |
| 2 | SINT_SMUX | 0 | R | SMUX Operation Interrupt. Indicates that SMUX command execution has finished. |
| 1:0 | Reserved | 0 | | Reserved |

10.2.6.5 STATUS 4 register (Address 0xBC)

Table 38: STATUS 4 register

| Addr: 0xBC | | STATUS 4 | | |
|------------|------------|----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | FIFO_OV | 0 | R | FIFO Buffer Overflow. Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read |
| 6 | Reserved | 0 | R | Reserved |
| 5 | OVTEMP | 0 | R | Over Temperature Detected. Indicates the device temperature is too high. Write 1 to clear this bit. |
| 4 | FD_TRIG | 0 | R | Flicker Detect Trigger Error. Indicates that there is a timing error that prevents flicker detect from working correctly. |
| 3 | Reserved | 0 | | Reserved |
| 2 | ALS_TRIG | 0 | R | ALS Trigger Error. Indicates that there is a timing error. The WTIME is too short for the selected ATIME. |
| 1 | SAI_ACTIVE | 0 | R | Sleep after Interrupt Active. Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit. |
| 0 | INT_BUSY | 0 | R | Initialization Busy. Indicates that the device is initializing. This bit will remain 1 for about 300 µs after power on. Do not interact with the device until initialization is complete. |

10.2.6.6 FD_STATUS register (Address 0xE3)

Table 39: FD_STATUS register

| Addr: 0xE3 | | FD_STATUS | | |
|------------|------------------------|-----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:6 | Reserved | | | Reserved |
| 5 | FD_MEASUREMENT_VALID | 0 | R | Flicker Detection Measurement Valid. Indicates that flicker detection measurement is complete. Write 1 to this bit to clear this field. |
| 4 | FD_SATURATION_DETECTED | 0 | R | Flicker Saturation Detected. Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field. |
| 3 | FD_120Hz_FLICKER_VALID | 0 | R | Flicker Detection 120 Hz Flicker Valid. Indicates that the 120 Hz flicker detection calculation is valid. Write 1 to this bit to clear this field. |
| 2 | FD_100Hz_FLICKER_VALID | 0 | R | Flicker Detection 100 Hz Flicker Valid. Indicates that the 100 Hz flicker detection calculation is valid. Write 1 to this bit to clear this field. |
| 1 | FD_120Hz_FLICKER | 0 | R | Flicker Detected at 120 Hz. Indicates if an ambient light source is flickering at 120 Hz. |
| 0 | FD_100Hz_FLICKER | 0 | R | Flicker Detected at 100 Hz. Indicates if an ambient light source is flickering at 100 Hz. |

10.2.7 ALS data and status

The ASTATUS register provides saturation and gain status associated to each set of ALS data. Reading the ASTATUS register (0x94) latches all 36 ALS data bytes to that status read. Reading these bytes consecutively (0x94 to 0xB8) ensures that the data is concurrent. All ALS data are stored as 16-bit values. If flicker detection is enabled, ALS channel five (CH5 ADC) is used for the flicker detection function. The ASTATUS and ALS data registers are read only.

10.2.7.1 ASTATUS register (Address 0x94)

Table 40: ASTATUS register

| Addr: 0x94 | | ASTATUS | | |
|------------|--------------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | ASAT_STATUS | 0 | R, SC | Saturation Status. Indicates if the latched data is affected by analog or digital saturation. |
| 6:4 | Reserved | 0 | R | Reserved |
| 3:0 | AGAIN_STATUS | 0 | R, SC | Gain Status. Indicates the gain applied for the ALS data latched to this ASTATUS read. |

10.2.7.2 DATA register (Address 0x95/0xB8)

Table 41: DATA_L register

| Addr: 0x95/97/99..B7 | | DATA_L | | |
|----------------------|----------|---------|--------|---------------------|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | DATA_L | 0 | R | ALS Data – low byte |

Table 42: DATA_H register

| Addr: 0x96/98/9A..B8 | | DATA_H | | |
|----------------------|----------|---------|--------|----------------------|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | DATA_H | 0 | R | ALS Data – high byte |

10.2.8 Miscellaneous configuration

10.2.8.1 CFG0 register (Address 0xBF)

Table 43: CFG0 register

| Addr: 0xBF | | CFG0 | | |
|------------|-----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7:6 | Reserved | 0 | | Reserved |
| 5 | LOW_POWER | 0 | RW | Low Power Idle. When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled. |
| 4 | REG_BANK | 0 | RW | Register Bank Access 0: Register access to register 0x80 and above. 1: Register access to register 0x20 to 0x7F. Note: Bit needs to be set to access registers 0x20 to 0x7F. If registers 0x80 and above needs to be accessed bit needs to be set to "0". |
| 3 | Reserved | 0 | | Reserved |
| 2 | WLONG | 0 | RW | Trigger Long. Increases the WTIME setting by a factor of 16. |
| 1:0 | Reserved | 0 | | Reserved |

10.2.8.2 CFG3 register (Address 0xC7)

Table 44: CFG3 register

| Addr: 0xC7 | | CFG3 | | |
|------------|----------|---------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:5 | Reserved | 0 | | Reserved |
| 4 | SAI | 0 | RW | Sleep After Interrupt. If set, the oscillator is turned off whenever an interrupt is active. SAI_ACTIVE is set in this event. To activate the oscillator again, clear all interrupts and clear the SAI_ACTIVE bit. |
| 3:0 | Reserved | 0xC | | Reserved |

10.2.8.3 CFG6 register (Address 0xF5)

Table 45: CFG6 register

| Addr: 0xF5 | | CFG6 | | | | | | | | | | | | |
|------------|---|---------|--------|---|-------|----------|---|---------------------------------|---|--|---|---|---|----------------------|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | |
| | | | | SMUX Command. Selects the SMUX command to execute when setting SMUXEN gets set. Do not change during ongoing SMUX operation. | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>VALUE</th> <th>SMUX_CMD</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ROM code initialization of SMUX</td> </tr> <tr> <td>1</td> <td>Read SMUX configuration to RAM from SMUX chain</td> </tr> <tr> <td>2</td> <td>Write SMUX configuration from RAM to SMUX chain</td> </tr> <tr> <td>3</td> <td>Reserved, do not use</td> </tr> </tbody> </table> | VALUE | SMUX_CMD | 0 | ROM code initialization of SMUX | 1 | Read SMUX configuration to RAM from SMUX chain | 2 | Write SMUX configuration from RAM to SMUX chain | 3 | Reserved, do not use |
| VALUE | SMUX_CMD | | | | | | | | | | | | | |
| 0 | ROM code initialization of SMUX | | | | | | | | | | | | | |
| 1 | Read SMUX configuration to RAM from SMUX chain | | | | | | | | | | | | | |
| 2 | Write SMUX configuration from RAM to SMUX chain | | | | | | | | | | | | | |
| 3 | Reserved, do not use | | | | | | | | | | | | | |
| 4:3 | SMUX_CMD | 2 | RW | | | | | | | | | | | |

10.2.8.4 CFG9 register (Address 0xCA)

Table 46: CFG9 register

| Addr: 0xCA | | CFG9 | | |
|------------|-----------|---------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | Reserved | 0 | | Reserved |
| 6 | SIEN_FD | 0 | RW | System Interrupt Flicker Detection. Enables system interrupt when flicker detection status change has occurred. |
| 5 | Reserved | | | Reserved |
| 4 | SIEN_SMUX | 0 | RW | System Interrupt SMUX Operation. Enables system interrupt when SMUX command has finished |
| 3:0 | Reserved | | | Reserved |

10.2.8.5 CFG20 register (Address 0xD6)

Table 47: CFG20 register

| Addr: 0xD6 | | CFG20 | | |
|------------|------------|---------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7 | FD_FIFO_8b | 0 | RW | <p>Enable 8-bit FIFO mode for Flicker Detection. 0: Disabled 1: Enabled Note: FD_TIME must be smaller than 256, else flicker data might be larger than 8 bits. In that case flicker data gets saturated to 0xFF.</p> |
| 6:5 | auto_smux | 0 | RW | <p>Automatic channel read-out 0: 6 Channel FZ, FY, FXL, NIR, 2xVIS, FD 1: Reserved 2: Automatic 12 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, FD Cycle 2: F2, F3, F4, F6, 2xVIS, FD 3: Automatic 18 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, FD Cycle 2: F2, F3, F4, F6, 2xVIS, FD Cycle 3: F1, F7, F8, F5, 2xVIS, FD Note: The bit “auto_smux” should only be changed before a measurement is started. Once a measurement is started, the device is automatically processing the channels as per definition above and storing the measurement results in the eighteen data registers. 2xVIS: Per default the “Top Left” and “Both Right” VIS/CLEAR PD is read-out.</p> |
| 4:0 | Reserved | | | Reserved |

10.2.8.6 PERS register (Address 0xCF)

Table 48: PERS register

| Addr: 0xCF | | PERS | | | | | | | | | | | | | | | | | | | | | | |
|------------|--|---------|--------|---|-------|---------|---|--|---|---|---|---|---|---|---|---|---|----|-----|-----------------|----|----|----|----|
| Bit | Bit name | Default | Access | Bit description | | | | | | | | | | | | | | | | | | | | |
| 7:4 | Reserved | 0 | | Reserved | | | | | | | | | | | | | | | | | | | | |
| 3:0 | APERS | 0 | RW | <p>ALS Interrupt Persistence. Defines a filter for the number of consecutive occurrences that ALS data must remain outside the threshold range between ALS_TH_L and ALS_TH_H before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>CHANNEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Every ALS cycle generates an interrupt</td> </tr> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>2</td> <td>2</td> </tr> <tr> <td>3</td> <td>3</td> </tr> <tr> <td>4</td> <td>5</td> </tr> <tr> <td>5</td> <td>10</td> </tr> <tr> <td>...</td> <td>5 x (APERS – 3)</td> </tr> <tr> <td>14</td> <td>55</td> </tr> <tr> <td>15</td> <td>60</td> </tr> </tbody> </table> | VALUE | CHANNEL | 0 | Every ALS cycle generates an interrupt | 1 | 1 | 2 | 2 | 3 | 3 | 4 | 5 | 5 | 10 | ... | 5 x (APERS – 3) | 14 | 55 | 15 | 60 |
| VALUE | CHANNEL | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Every ALS cycle generates an interrupt | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 2 | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 10 | | | | | | | | | | | | | | | | | | | | | | | |
| ... | 5 x (APERS – 3) | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 55 | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | 60 | | | | | | | | | | | | | | | | | | | | | | | |

10.2.9 FIFO buffer data and status

The FIFO buffer is used to poll ALS data with fewer I²C read and write transactions. The FIFO buffer is 256 bytes of RAM containing 128 two-byte datasets. If the FIFO overflows (i.e. 129 datasets before host reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. The Host acquires data by reading addresses: 0xFE – 0xFF. The register address pointer automatically wraps from 0xFF to 0xFE as data are read. Data can be read one byte at a time or in blocks, (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL update for each two-byte entry. If the FIFO continues to be accessed after FIFO_LVL = 0, the device will return 0 for all data. The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO_LVL.

10.2.9.1 FIFO_MAP register (Address 0xFC)

Table 49: FIFO_MAP register

| Addr: 0xFC | | FIFO_MAP | | |
|------------|---------------------|----------|--------|---|
| Bit | Bit name | Default | Access | Bit description |
| 7 | Reserved | 0 | | Reserved |
| 6 | FIFO_WRITE_CH5_DATA | 0 | RW | <p>FIFO Write CH5 Data. If set, CH5 data is written to the FIFO Buffer. (two bytes per sample) Note: If flicker detection is enabled, this bit is ignored. Refer to register 0xD7 for FDEN="1".</p> |
| 5 | FIFO_WRITE_CH4_DATA | 0 | RW | <p>FIFO Write CH4 Data. If set, CH4 data is written to the FIFO Buffer. (two bytes per sample).</p> |
| 4 | FIFO_WRITE_CH3_DATA | 0 | RW | <p>FIFO Write CH3 Data. If set, CH3 data is written to the FIFO Buffer. (two bytes per sample).</p> |
| 3 | FIFO_WRITE_CH2_DATA | 0 | RW | <p>FIFO Write CH2 Data. If set, CH2 data is written to the FIFO Buffer. (two bytes per sample).</p> |
| 2 | FIFO_WRITE_CH1_DATA | 0 | RW | <p>FIFO Write CH1 Data. If set, CH1 data is written to the FIFO Buffer. (two bytes per sample).</p> |
| 1 | FIFO_WRITE_CH0_DATA | 0 | RW | <p>FIFO Write CH0 Data. If set, CH0 data is written to the FIFO Buffer. (two bytes per sample).</p> |
| 0 | FIFO_WRITE_ASTATUS | 0 | RW | <p>FIFO Write Status. If set, ASTATUS (one byte per sample) is written to the FIFO Buffer.</p> |

10.2.9.2 FIFO_CFG0 register (Address 0xDF)

Table 50: FIFO_CFG0 register

| Addr: 0xDF | | FIFO_CFG0 | | |
|------------|---------------|-----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7 | FIFO_WRITE_FD | 0 | RW | <p>FIFO Write Flicker Detection If set flicker raw data is written into FIFO (one byte per sample). Note: This bit is ignored if flicker detection is disabled. Refer to register 0xFC for FDEN="0".</p> |
| 6:0 | Reserved | 0100001 | | Reserved, do not change. |

10.2.9.3 FIFO_LVL register (Address 0xFD)

Table 51: FIFO_LVL register

| Addr: 0xFD | | FIFO_LVL | | |
|------------|----------|----------|--------|--|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | FIFO_LVL | 0 | R | FIFO Buffer Level. Indicates the number of entries (each are 2 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256 byte, the FIFO_LVL range is from 0 entries to 128 entries. |

10.2.9.4 FDATA register (Address 0xFE and 0xFF)

Table 52: FDATA_L register

| Addr: 0xFE | | FDATA_L | | |
|------------|----------|---------|--------|------------------|
| Bit | Bit name | Default | Access | Bit description |
| 7:0 | FDATA | 0 | R | FIFO Buffer Data |

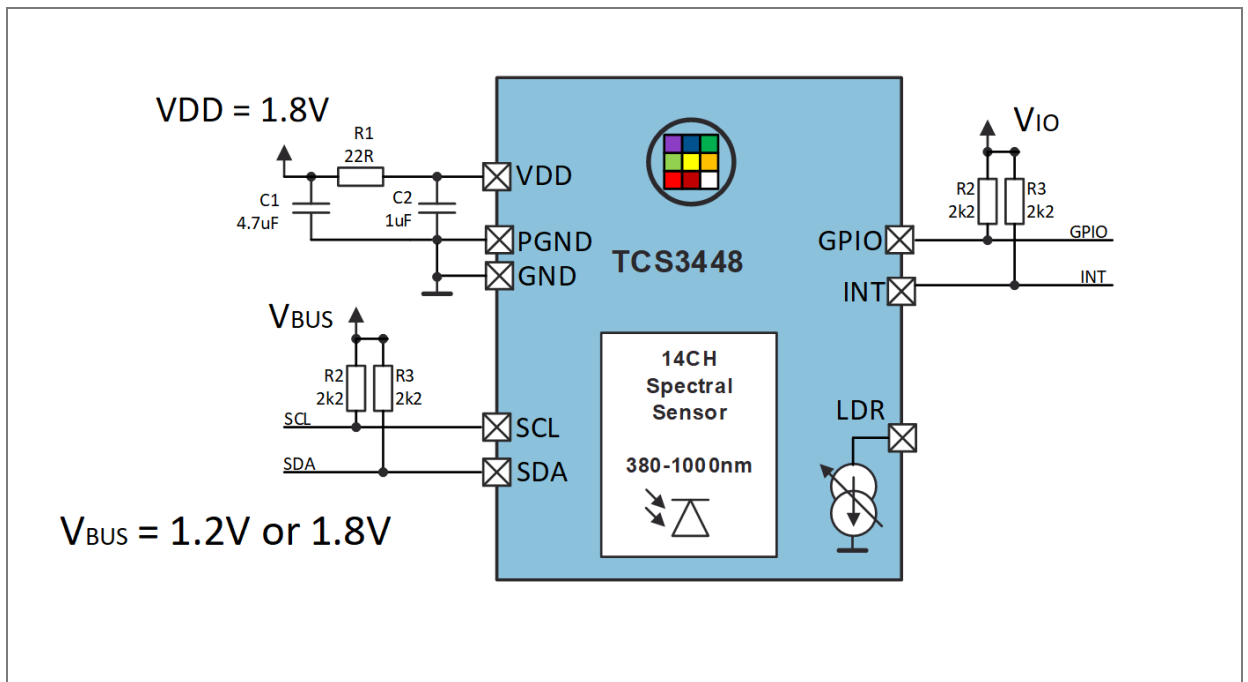
Table 53: FDATA_H register

| Addr: 0xFF | | FDATA_H | | |
|------------|----------|---------|--------|------------------|
| Bit | Bit name | Default | Access | Bit description |
| 15:8 | FDATA | 0 | R | FIFO Buffer Data |

11 Application information

11.1 Schematic

Figure 10: Application example



Pin GPIO is used to select the I²C bus interface voltage during start-up of the device. Please refer to chapter “Selection of I²C bus interface voltage” for details.

Configuration examples:

$V_{GPIO} = GND : V_{BUS} = 1.2 V$

$V_{GPIO} = 1.2 V : V_{BUS} = 1.2 V$

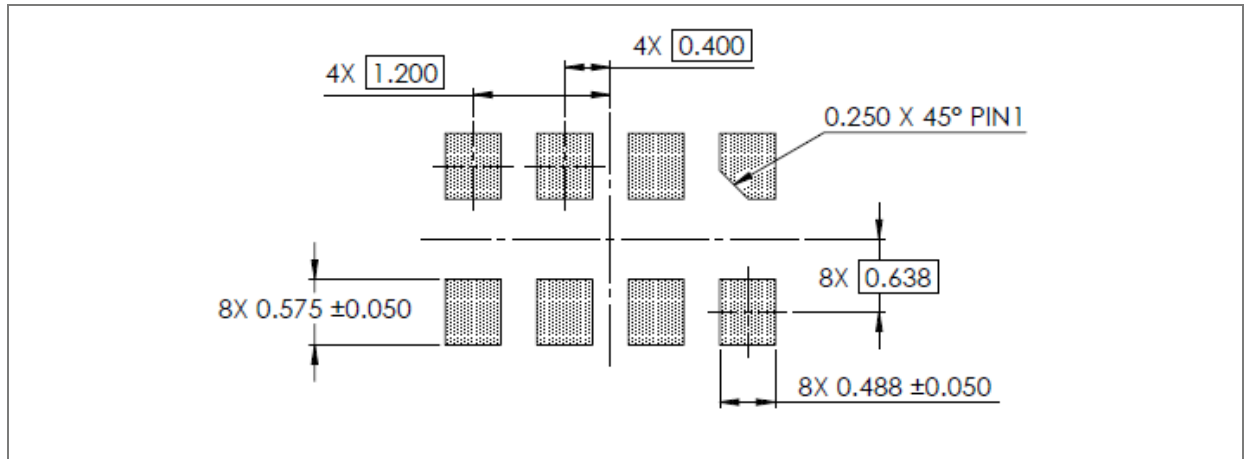
$V_{GPIO} = 1.8 V : V_{BUS} = 1.8 V$

$V_{GPIO} = 3.3 V : V_{BUS} = 1.8 V$

Pins GPIO and INT are both 3 V compliant (3.6 V abs max) and do not have to be connected to the same V_{IO} voltage.

11.2 PCB pad layout

Figure 11: Recommended PCB pad layout

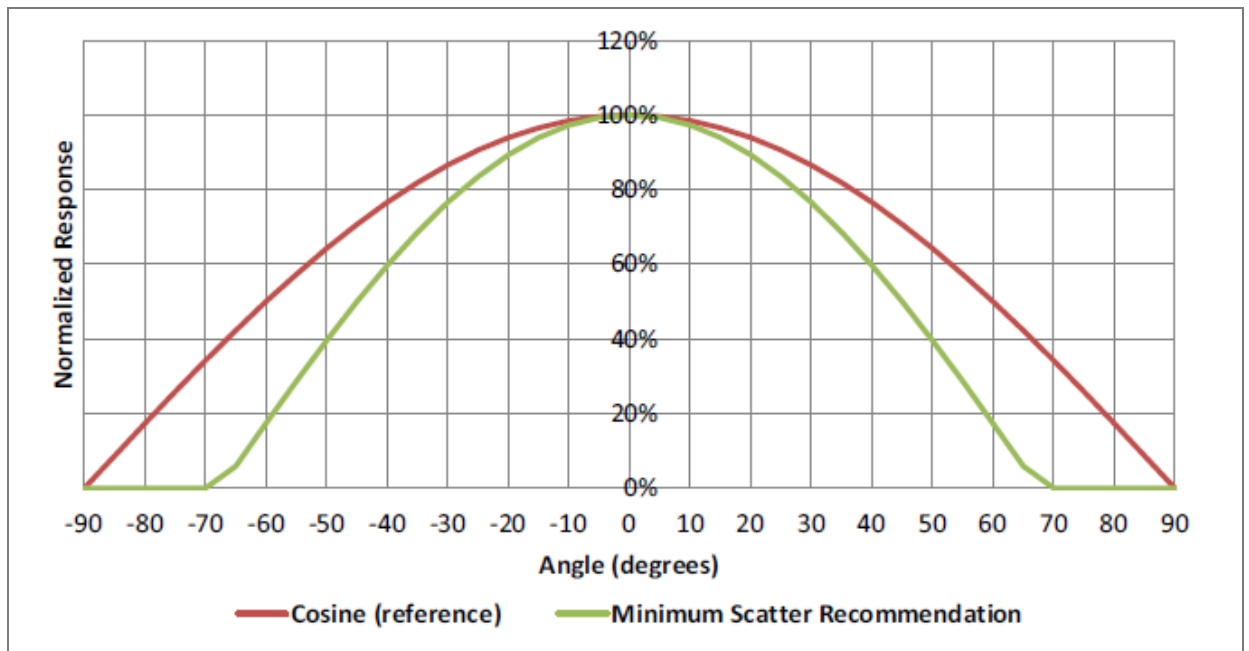


- (1) All dimensions are in millimeters.
- (2) Dimension tolerances are 0.05 mm unless otherwise noted.
- (3) This drawing is subject to change without notice.

11.3 Application optical requirements

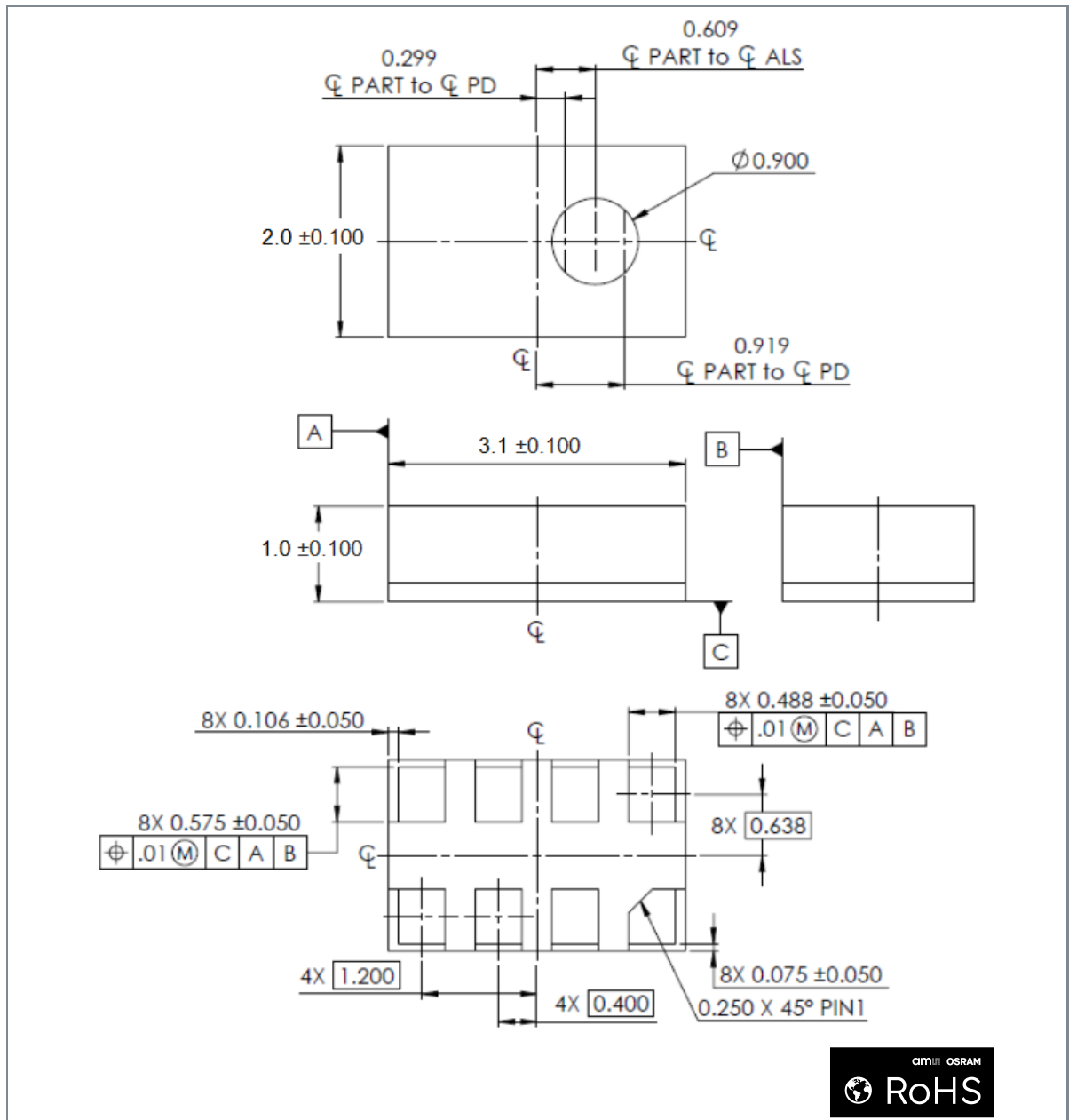
For stable performance, an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the optical design guide or contact ams OSRAM.

Figure 12: Diffuser characteristics



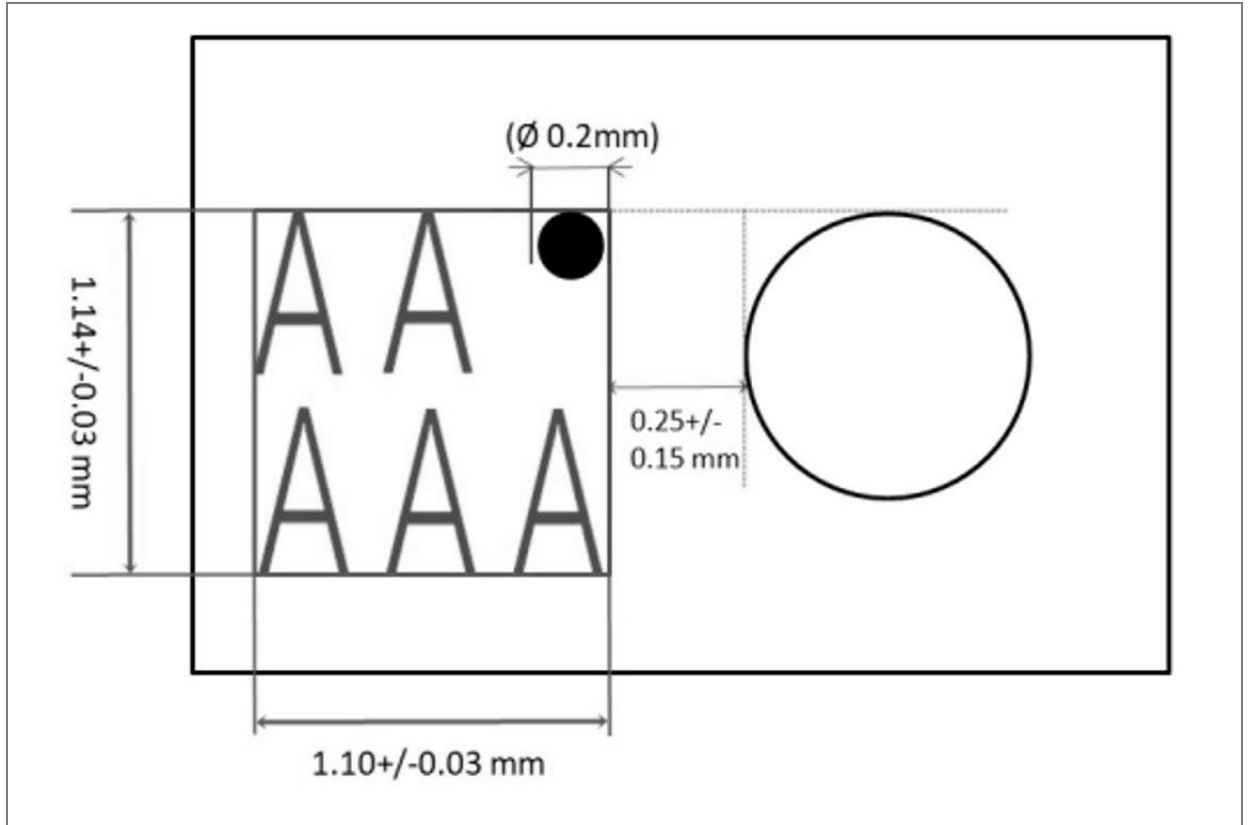
12 Package drawings & markings

Table 54: OLGA8 package outline drawing



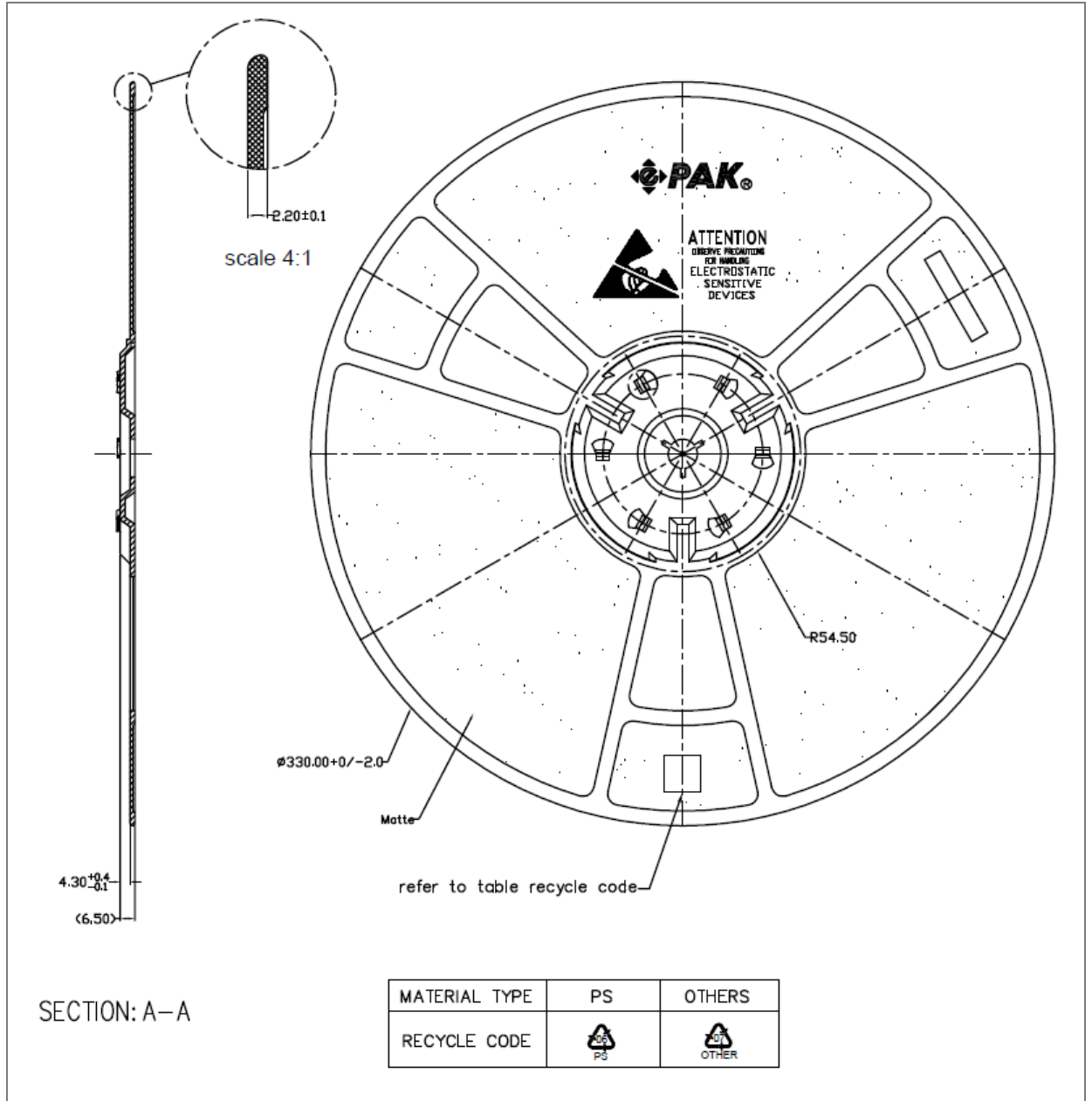
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
- (3) This package contains no lead (Pb).
- (4) This drawing is subject to change without notice.

Figure 13: OLGA8 package marking



- (1) Marking code consists of random characters or digits. Placeholder is indicated with "AAAAA" in drawing.
- (2) All dimensions are in millimeters. Angles in degrees.
- (3) Dimensioning and tolerance conform to ASME Y14.5M-1994.
- (4) This package contains no lead (Pb).
- (5) This drawing is subject to change without notice.

Figure 15: TCS3448 OLGA8 reel dimensions



- (1) All dimensions are in millimeters. Angles in degrees.
- (2) This drawing is subject to change without notice.

14 Soldering & storage information

The module has been tested and has demonstrated an ability to be reflow-soldered to a PCB substrate. Please observe, however, that such repeated temperature stress may alter measurements results and optical performance and will influence color measurement accuracy. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 16: Solder reflow profile graph

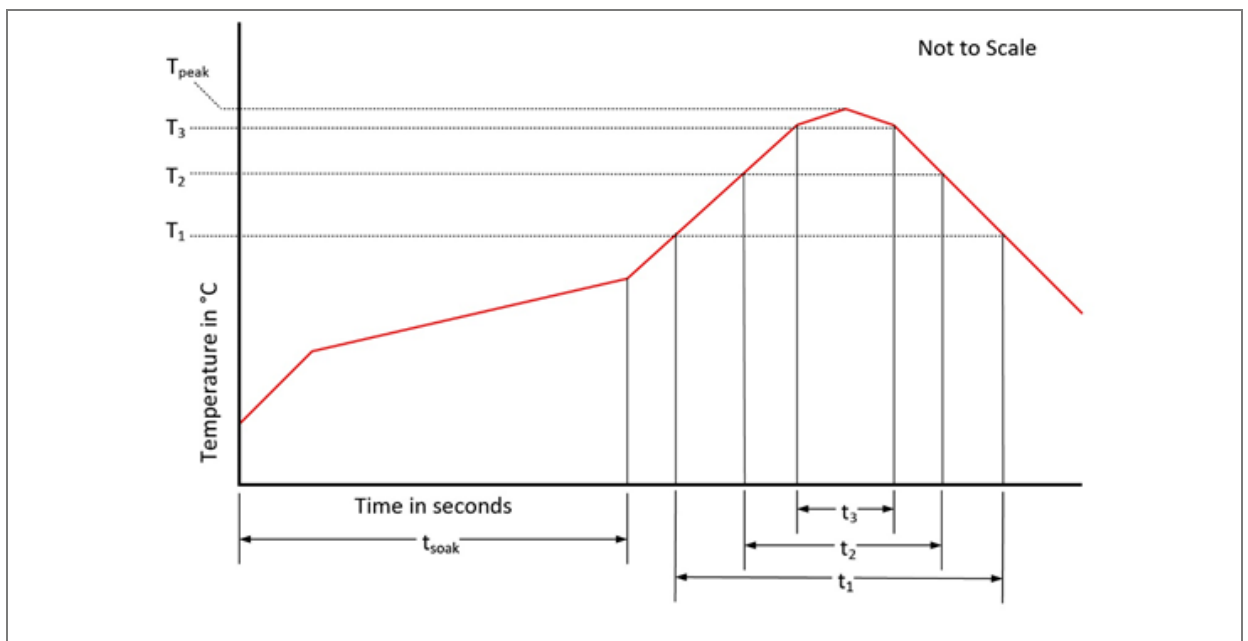


Table 55: Solder reflow profile

| Parameter | Reference | Device |
|--|------------|----------------|
| Average temperature gradient in preheating | | 2.5 °C/s |
| Soak time | t_{soak} | 2 to 3 minutes |
| Time above 217 °C (T1) | t_1 | Max 60 s |
| Time above 230 °C (T2) | t_2 | Max 50 s |
| Time above $T_{peak} - 10$ °C (T3) | t_3 | Max 10 s |
| Peak temperature in reflow | T_{peak} | 260 °C |
| Temperature gradient in cooling | | Max -5 °C/s |

14.1 Storage information

14.1.1 Moisture sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

14.1.2 Shelf life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90%

Re-baking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region. Please observe, however, that such repeated temperature stress may alter measurements results and optical performance and will influence color measurement accuracy.

14.1.3 Floor life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30 °C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be re-baked prior to solder reflow or dry packing. Please observe, however, that such repeated temperature stress may alter measurements results and optical performance and will influence color measurement accuracy.

14.1.4 Re-baking instructions

When the shelf life or floor life limits have been exceeded, re-bake at 50 °C for 12 hours.

15 Revision information

| Document status | Product status | Definition |
|-----------------------|-----------------|---|
| Product Preview | Pre-development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
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| Changes from previous released version to current revision v2-00 | Page |
|--|------|
| Updated ordering information | 7 |
| Changed irradiance responsivity limits | 13 |

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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